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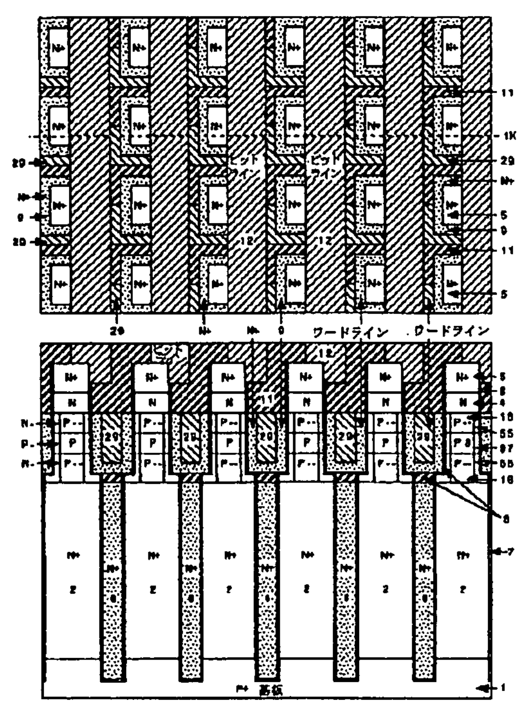
(54)【発明の名称】　超高密度集積回路

(57)【要約】　（修正有）

【課題】ＤＲＡＭなどのアレイにおいて、高密度化とパフォーマンスの向上を図る。

【解決手段】不等方性エッチング、側壁スペーサ、ＲＩＥの組合せで相対的に浅いトレンチと深いトレンチを形成し、メモリセルのための埋込みビットライン（ＢＢＬ）セル構造と、ＤＲＡＭのアクセス・トランジスタ、ＳＲＡＭ、周辺ＣＭＯＳなどのための埋込みゲート・トランジスタ（ＢＧＴ）を形成する。各トランジスタは同じゲートとチャネル長でシングルチップ上に集積することができる。ビットライン１２はメタル、ポリシリコン、またはポリサイドからなり、上部とサイドのコンタクトであるため、５０％近いミスアラインメントでも影響を受けない。ワードラインはゲートの側壁ポリシリコン９とメタル２９からなり、垂直位置が十分低くなっているためビットラインと短絡することがない。



【外国語明細書】

1 Title of Invention

ULTRA DENSE INTEGRATED CIRCUITS

2 Claims

1. A conductive line including conductive films surrounding the sidewalls of a plurality of semiconductor devices, and conductive films under patterned materials at bottom of the grooves.

2. A conductive line according to claim 1 wherein said semiconductor devices are vertical field-effect transistors.

3. A conductive line according to claim 1 wherein said conductive films are much lower than the top parts of said semiconductor devices.

4. A conductive line according to claim 1 wherein said patterned materials are conductive and said patterned materials are not only a patterning mask of said conductive films but also a part of said conductive line to reduce the resistance of said conductive line.

5. A conductive line according to claim 4 wherein said conductive films and said patterned materials are much lower than the top parts of said semiconductor devices.

6. A basic structure comprising:

a first semiconductor;

a second semiconductor on said first semiconductor; a third heavily doped semiconductor on said second semiconductor;

a fourth semiconductor on said first semiconductor; a fifth heavily doped semiconductor on said fourth semiconductor;

a dielectric dividing said second, third, fourth, and fifth semiconductors into a plurality of regions;

a plurality of semiconductor devices on said third and fifth semicondctors, respectively;

a plurality of conductive lines including conductive films surrounding the sidewalls of said

semiconductor devices, and conductive films under patterned materials at bottom of the grooves.

7. A basic structure according to claim 6 wherein the vertical dimensions of said dielectric in some areas are different.

8. A conductive line according to claim 6 wherein said conductive films are much lower than the top parts of said semiconductor devices.

9. A basic structure according to claim 6 wherein said first semiconductor is heavily doped.

10. A basic structure according to claim 6 wherein said second semiconductor is lightly doped.

11. The fourth secomductor of claim 6, further including a relatively high doping semiconductor and a relatively low doping semiconductor.

12. A basic structure according to claim 6 wherein said second and fifth semiconductors have the same conductivity type as said first semiconductor and said third and fourth semiconductors have the opposite conductivity type as said first semiconductor.

13. The basic structure of claim 6, producing ultra dense dynamic random access memory arrays with a minimum 4 lithographic squares cell size, ultra dense full single crystal semiconductor 6-T static random access memory arrays with a minimum 40 lithographic squares cell size, and extremely high density logic circuits.

14. A basic structure comprising:

a first semiconductor;

a second semiconductor on said first semiconductor;

a third semiconductor on said second semiconductor;

a fourth semiconductor on said second semiconductor; a fifth semiconductor on said fourth semiconductor;

a sixth semiconductor on said second semiconductor; a seventh semiconductor on said sixth semiconductor;

a surrounding material dividing said second, third, fourth, fifth, sixth, and seventh semiconductors into a plurality of regions;

a plurality of semiconductor devices on said third, fifth, and seventh semicondctors, respectively;

a plurality of conductive lines including conductive films surrounding the sidewalls of said semiconductor devices, and conductive films under patterned materials at bottom of the grooves.

15. A basic structure according to claim 14 wherein the vertical dimensions of said surrounding material in some areas are different.

16. The surrounding material of claim 14, further including a thin insulative film, a dielectric, and an eighth semiconductor.

17. A surrounding material according to claim 16 wherein said dielectric is on said eighth semiconductor.

18. A basic structure according to claim 14 wherein said conductive films are much lower than the top parts of said semiconductor devices.

19. A basic structure according to claim 14 wherein said first semiconductor is heavily doped.

20. A basic structure according to claim 14 wherein said second semiconductor is heavily doped.

21. A basic structure according to claim 14 wherein said third semiconductor is heavily doped.

22. The fourth secomductor of claim 14, further including a relatively high doping semiconductor and a relatively low doping semiconductor.

23. A basic structure according to claim 14 wherein said fifth and seventh semiconductors are heavily doped and said sixth semiconductor is lightly doped.

25. A basic structure according to claim 13 wherein said fourth and seventh semiconductors have the same conductivity type as said first semiconductor and said second, third, fifth, and sixth semiconductors have the opposite conductivity type as said first semiconductor.

26. The basic structure of claim 13, producing ultra dense dynamic random access memory arrays with a minimum of 4 lithographic squares cell size, ultra dense full single crystal semiconductor 6-T static random access memory arrays with a minimum of 40 lithographic squares cell size, and extremely high density logic circuits.

27. A basic structure comprising:

a conductive film surrounding about half of a semiconductor island;

a plurality of said conductive films self-aligned connecting together to form conductive lines;

thin dielectric film between said conductive film and semiconductor island.

28. A basic structure according to claim 27 wherein said conductive films are much lower than the top parts of said semiconductor islands.

29. A basic structure comprising:

conductive films surrounding semiconductor islands and disconnecting each other;

thin dielectric film between said conductive film and semiconductor island;

dielectrics surrounding said conductive films;

conductive materials, one of which connecting said two conductive films to form a conductive line, disconnecting each other.

30. A basic structure according to claim 29 wherein said conductive films and conductive materials are much lower than the top parts of said semiconductor islands.

31. An ultra dense dynamic random access memory array comprising:

a substrate;

a plurality of storage nodes, surrounded by a cell plate and dielectrics for capacitors;

a plurality of semiconductor devices;

a plurality of word lines including conductive films surrounding the sidewalls of said semiconductor devices, and conductive films under patterned materials at bottom of the grooves;

a plurality of bit lines.

32. An ultra dense dynamic random access memory array according to claim 31 wherein some parts of said bit lines are on said semiconductor devices and the other parts of bit lines stick to the sidewalls of said semiconductor devices.

33. An ultra dense dynamic random access memory array according to claim 31 wherein said conductive films are much lower than said bit lines.

34. An ultra dense dynamic random access memory array according to claim 31 wherein said patterned materials are conductive and said patterned materials are not only a patterning mask of said conductive films but also a part of said word lines to reduce the resistance of said word lines.

35. An ultra dense dynamic random access memory array according to claim 34 wherein said conductive films and said patterned materials are much lower than said bit lines.

36. An ultra dense dynamic random access memory array according to claim 31 wherein the area of the horizontal cross section of the active region of said semiconductor device is smaller than one minimum lithographic square and the area of the horizontal cross section of said storage node is larger than one minimum lithographic square.

37. An ultra dense dynamic random access memory array according to claim 31 wherein said substrate and storage nodes are heavily doped semiconductors.

38. The ultra dense dynamic random access memory array of claim 31, further including a dielectric between said conductive films and cell plates.

39. An ultra dense dynamic random access memory array according to claim 31 wherein the channel length and threshold voltage of said semiconductor devices are determined by ion-implantation.

40. An ultra dense dynamic random access memory array according to claim 31 wherein the channel length of said semiconductor device is determined by two ion implants.

41. An ultra dense dynamic random access memory array according to claim 31 wherein the channel length of said semiconductor device is only determined by one ion implant when the doping profile of said ion implant is used.

42. An ultra dense dynamic random access memory array according to claim 31 wherein said conductive films are used as a doping mask to form shallow source and drain extension regions of said semiconductor devices.

43. An ultra dense dynamic random access memory array according to claim 31 wherein said storage nodes are pillar-shaped.

44. An ultra dense dynamic random access memory array according to claim 31 wherein said storage nodes are tube-shaped.

45. An ultra dense dynamic random access memory array according to claim 44 wherein the doping concentrations of the outside and inside surfaces of said tube-shaped storage nodes are different.

46. Bit lines of an ultra dense dynamic random access memory array below all transistors including access transistors and logic transistors.

47. Storage nodes of an ultra dense dynamic random access memory array, made from multiple-level interconnect and contact materials.

48. The storage nodes of claim 47, completely surrounded by insulating materials.

49. The storage nodes of claim 47, occupying almost all the area of said dynamic random

access memory array.

50. Storage nodes according to claim 47 wherein the spacing between said two neighboring storage nodes is much smaller than a minimum lithographic line width.

51. Storage nodes according to claim 47 wherein said storage nodes are pillar-shaped.

52. Storage nodes according to claim 47 wherein said storage nodes are tube-shaped.

53. Storage nodes of an ultra dense dynamic random access memory array, made from multiple-level interconnect materials.

54. Storage nodes of an ultra dense dynamic random access memory array, made from multiple-level contact materials.

55. A part of a storage node of an ultra dense dynamic random access memory array, made from multiple-level interconnect and contact materials.

56. A part of a storage node of an ultra dense dynamic random access memory array, made from multiple-level interconnect materials.

57. A part of a storage node of an ultra dense dynamic random access memory array, made from multiple-level contact materials.

58. Both horizontal doping profile and vertical doping profile, not uniform between heavily doped source and drain regions of a vertical field-effect transistor.

59. The vertical field-effect transistor of claim 59, including relatively low doping body regions, a relatively high doping body region, a relatively low doping channel region, and shallow source and drain extension regions between said heavily doped source and drain regions.

60. The vertical field-effect transistor of claim 59, including relatively low doping body regions, a relatively high doping body region, a relatively low doping buried channel region, and shallow source and drain extension regions between said heavily doped source and drain regions.

174. A basic structure comprising:

a substrate;

a plurality of semiconductor islands disposed on said substrate;

a conductive film surrounding each of said plurality of semiconductor islands,

wherein said conductive film is patterned to form a plurality of conductive lines;

a patterned material,

wherein said patterned material is conductive and said patterned material is not only a patterning mask of said conductive film but also a part of each of said plurality of conductive lines to reduce a resistance of each of said plurality of conductive lines;

an insulating film between said conductive film and each of said plurality of semiconductor islands.

175. A basic structure according to claim 174 wherein said plurality of semiconductor islands are a plurality of vertical field-effect transistors and said conductive film is not only a gate electrode of each of said plurality of vertical field-effect transistors but also a doping mask of source and drain extension regions of said plurality of vertical field-effect transistors.

176. The basic structure of claim 174, further forming a dynamic random access memory array.

177. The basic structure of claim 174, further forming a static random access memory array.

180. A basic structure comprising:

a conductive film surrounding a semiconductor island;

a dielectric film between said conductive film and said semiconductor island,

wherein said semiconductor island is a vertical field-effect transistor, said conductive film is a gate electrode of said vertical field-effect transistor, and said dielectric film is a gate

insulator of said vertical field-effect transistor,

wherein both horizontal doping profile and vertical doping profile are not uniform between heavily doped source and drain regions of said vertical field-effect transistor.

181. The vertical field-effect transistor of claim 180, including low doping body regions, a high doping body region, a low doping channel region, and source and drain extension regions between said heavily doped source and drain regions.

182. The vertical field-effect transistor of claim 180, including low doping body regions, a high doping body region, a low doping buried channel region, and source and drain extension regions between said heavily doped source and drain regions.

183. The basic structure of claim 180, further forming a dynamic random access memory array.

184. The basic structure of claim 180, further forming a static random access memory array.

185. A basic structure comprising:

a substrate;

a plurality of semiconductor islands disposed on said substrate;

a conductive film surrounding each of said plurality of semiconductor islands,

wherein said conductive film is patterned to form a plurality of conductive lines;

a dynamic random access memory array,

wherein said dynamic random access memory array includes a plurality of different doping concentrations of storage nodes;

an insulating film between said conductive film and each of said plurality of semiconductor islands.

186. A basic structure comprising:

a substrate;

a plurality of semiconductor islands disposed on said substrate;

a conductive film surrounding each of said plurality of semiconductor islands,

wherein said conductive film is patterned to form a plurality of conductive lines;

a dynamic random access memory array,

wherein said dynamic random access memory array includes a plurality of tube-shaped storage nodes,

wherein each of said plurality of tube-shaped storage nodes includes a plurality of different doping concentrations of semiconductors;

an insulating film between said conductive film and each of said plurality of semiconductor islands.

187. A basic structure comprising:

a substrate;

a plurality of semiconductor islands disposed on said substrate;

a plurality of conductive films disposed on said substrate,

wherein each of said plurality of conductive films less than 360 degrees encircles each of said plurality of semiconductor islands,

wherein said plurality of conductive films self-aligned connect together to form a plurality of conductive lines,

wherein said plurality of conductive lines are separated each other;

an insulating film between each of said plurality of conductive films and each of said plurality of semiconductor islands,

wherein each of said plurality of semiconductor islands includes a vertical field-effect transistor,

wherein each of said plurality of conductive films is a gate electrode of said vertical field-effect transistor,

wherein said insulating film is a gate insulator of said vertical field-effect transistor,

wherein both horizontal doping profile and vertical doping profile are not uniform between heavily doped source and drain regions of said vertical field-effect transistor.

188. The vertical field-effect transistor of claim 187, including low doping body regions, a high doping body region, a low doping channel region, and source and drain extension regions between said heavily doped source and drain regions.

189. The vertical field-effect transistor of claim 187, including low doping body regions, a high doping body region, a low doping buried channel region, and source and drain extension regions between said heavily doped source and drain regions.

190. A basic structure comprising:

a substrate;

a plurality of semiconductor islands disposed on said substrate;

a plurality of conductive films disposed on said substrate,

wherein each of said plurality of conductive films less than 360 degrees encircles each of said plurality of semiconductor islands,

wherein said plurality of conductive films self-aligned connect together to form a plurality of conductive lines,

wherein said plurality of conductive lines are separated each other;

an insulating film between each of said plurality of conductive films and each of said plurality of semiconductor islands;

a dynamic random access memory array,

wherein said plurality of conductive lines are word lines of said dynamic random access memory array;

a patterned material,

wherein said patterned material is conductive and said patterned material is not only a patterning mask of said plurality of conductive films but also a part of each of said word lines to reduce a resistance of each of said word lines.

191. A basic structure according to claim 190 wherein said dynamic random access memory

array includes a plurality of bit lines and semiconductor devices.

192. A basic structure according to claim 191 wherein some parts of said plurality of bit lines are on said plurality of semiconductor islands and the other parts of said plurality of bit lines adhere to sidewalls of said plurality of semiconductor islands.

193. A basic structure according to claim 190 wherein said dynamic random access memory array includes a plurality of two-level bit lines.

194. A basic structure comprising:

a substrate;

a plurality of semiconductor islands disposed on said substrate;

a plurality of conductive films disposed on said substrate,

wherein each of said plurality of conductive films less than 360 degrees encircles each of said plurality of semiconductor islands,

wherein said plurality of conductive films self-aligned connect together to form a plurality of conductive lines,

wherein said plurality of conductive lines are separated each other;

an insulating film between each of said plurality of conductive films and each of said plurality of semiconductor islands;

a patterned material,

wherein said patterned material is conductive and said patterned material is not only a patterning mask of said plurality of conductive films but also a part of each of said plurality of conductive lines to reduce a resistance of each of said plurality of conductive lines.

3 Detailed Description of Invention

FIELD OF THE INVENTION

This invention relates, in general, to semiconductor device structures, interconnect methods, and fabrication techniques, and in particular, to ultra dense memory arrays and the methods of fabrication.

BACKGROUND OF THE INVENTION

MOS integrated circuit technologies have made tremendous progress within a very short period of time. Especially within the last two decades when semiconductor memories started to replace conventional magnetic core memories, progress in integration density has increased at an extremely high rate. MOS random access memories (RAMs) devices have played a very important role in developing the new generation of fabrication technology. This is due to the fact that memory device have high regularity, which is a great advantage in developing new processing technology. In addition, the fact that there exists quite a large market for memory devices allowing a large amount of resources to be invested results in very strong competition in research and development. The fabrication technology introduced by the development of RAMs has been transferred to a variety of

fabrication products.

There are dynamic and static RAMs. Dynamic RAMs (DRAMs) store charge on a capacitor and static RAMs (SRAMs) use a latch to store data. In CMOS, a latch is commonly formed by two cross-coupled inverters. The one-transistor (1-T) DRAM cell is most attractive for high density memory arrays due to the smaller cell area. Both DRAMs and SRAMs are key components in computer systems and supporting progress in data processing systems.

Applications demanding greater speed in new generation computers demand a corresponding increase in memory size to effectively utilize those speed improvements. The addition of low density chips to increase memory size can have an adverse effect on the reliability of the system. For this reason, DRAM designers have been driven to achieve smaller size of a cell in new cell designs. In addition to improving performance and reliability, the decreased size of a cell reduces the size, price and weight of the overall system.

In order to realize high density DRAMs, many leading semiconductor manufacturers have launched very strongly competing cell structure innovations in the world; a number of memory cell structures, such as trench capacitor cells and stacked capacitor cells, have been developed. However, further down-scaling of these cells would hardly satisfy both the cell area and storage capacitance requirements toward 256 Mbit and beyond. Some new three-dimensional memory cells which are named 1-F (feature size) cell, 2-F cell, and 4-F cell are proposed in the second invention. They can achieve an incredibly small cell size of a minimum 1-4 lithographic squares and a large capacitance without cell leakage. For comparison, I give the following table for the most advanced DRAM cells in the world.

Company	DRAM Cell	Size of Cell (the number of minimum lithographic squares)
Fujitsu Ltd.	3-dimensional stacked capacitor cell	17.6
IBM	Commercial 16Mb DRAM cell	16.5
Mitsubishi Electric Corp.	Novel stacked capacitor cell with dual cell plate	14.4
NEC Corp.	Capacitor-over-bit-line cell with a hemispherical-grain storage node	14.4

Hitachi Ltd.	New stacked capacitor DRAM cell characterized by a storage capacitor on a bit-line structure	13.4
IBM	Buried-trench DRAM cell using a self -aligned epitaxy over trench technology	10.8
Toshiba Corp.	Asymmetrical stacked trench capacitor cell	9.6
Toshiba Corp.	Spread source/drain MOSFET using selective silicon growth	8.0
Toshiba Corp.	Surrounding gate transistor cell	7.2
Hui Lai	4-F cell	4.0
Hui Lai	2-F cell	2.0
Hui Lai	1-F cell	1.0

From the above table, we can see that the new DRAM cells in the second invention have the smallest cell area among all the cells in the world. This will lead to some great advantages. For example, using the 4-F cell, we can apply conventional optical lithographic technology for 64 Mbit DRAM production with a relaxed design rule of 0.6 μm; SEMATECH and other companies have to use deep-uv or phase-shift technology for 64 Mbit DRAM production with 0.35 μm design rule. Using the design rule of 64 Mbit DRAM (0.35 μm), the 4-F cell can achieve a cell area of 256 Mbit DRAM (0.5 μm^2). For the 1-F and 2-F cells, they can be used for multiple Gbit DRAMs. Therefore, the new cells will be able to pave the way to giga-bit DRAM era. This will make semiconductor memory devices replace rotating disc media (disk drivers) in the computer to lead to the next computer revolution. This will also lead to the development of the other new products and technology. For example, language-translation devices, intelligent devices, high-defination and interactive TV, high-defination video receivers/recorders, and storage systems require huge amounts of memory. If high-level language-translation devices are achieved, people do not need to spend time to learn many languages, more business opportunities outside the U.S. would be created, and people in different parts of the world would work more closely, sociably, and efficiently.

Although the DRAM cell can provide the highest density memory arrays, SRAM has a higher speed, a wider operational margin, higher reliability, and ease of use. In Mega-bit SRAMs, reducing the cell size and decreasing the supply voltage (V_{cc}), cause the level of a cell node which stores "high" to decrease. Therefore cell operation stability is becoming a serious problem. One of the solutions of this problem is to increase the cell ratio (b_D/b_A) by adopting a large size ratio ($(W_D/L_D)/(W_A/L_A)$) of a driver transistor to an access transistor. However, this is inconsistent with reducing cell size and is therefore unsuitable for Mega-bit SRAMs. Recently, another solution has been developed. Polycrystalline-silicon TFT (Thin Film Transistor) loads have been used instead of polycrystalline-silicon (poly-Si) resistors in order to obtain a high charging current and low leakage current for the cell node. However, the levels of on/off current of the poly-Si thin film transistor are not enough to solve the above problem for 64 Mbit SRAMs and beyond. If single-crystalline-silicon transistors are used instead of said poly-Si transistors, the problem of on/off current can be solved. However, the single-crystalline-silicon transistors could not be used as loads in the conventional cell structures of Mega-bit SRAMs because the poly-Si TFT loads are stacked on single-crystalline-silicon transistors to decrease cell areas. If single-crystalline-silicon transistors must be used as loads, all transistors have to be fabricated on the same level, but this leads to larger cell areas and lower density integrated circuits. Fortunately, the second invention overcomes this very difficult problem by using new cell structures. The new structures not only can achieve the smallest cell size for high density SRAM and the largest W/L ratio for high noise immunity in the world, but also use single-crystalline-silicon transistors as loads instead of the stacked poly-Si transistors to provide good transistor characteristics to solve the problem of on/off current. For comparison, I give the following table for the most advanced SRAM cells in the world.

Company	SRAM Cell	Size of Cell (the number of minimum lithographic squares)
Philips Research Lab.	0.5μm bulk full CMOS 6-T cell with fully overlapping contacts	100.8
Motorola Inc.	0.5μm BiCMOS triple poly-Si 4-T cell	100.0
Texas Instruments	0.5μm BiCMOS cell with a vertical NMOS driver transistor and a stacked poly-Si PMOS load device	92.0
Mitsubishi	A large cell-ratio and low node leak 16Mb	63.9

Electric Corp.	SRAM cell using ring-gate transistors. 0.35μm, retrograde twin well, quadruple poly-Si, double metal, stacked poly-Si PMOS.	
Fujitsu Ltd.	A split word line cell for 16Mb SRAM using polysilicon sidewall contacts. 0.4μm, twin well, quintuple poly, double metal, stacked poly-Si PMOS.	54.5
Hitachi Ltd.	A 5.9 μm^2 super low power SRAM cell using a new phase-shift lithography. 0.35μm, triple well, quadruple poly-Si, double metal, stacked poly-Si PMOS.	48.1
Hitachi Ltd.	0.6μm stacked poly-Si PMOS cell	47.2
NEC Corp.	16Mb SRAM cell using a self-aligned contact process. 0.4μm design rule.	45.0
Hui Lai	Full single crystal Si 6-T cell. SRAM process is completely compatible to DRAM and CMOS logic circuit process.	40.0

The third great advantage of the second invention is that memory circuits (DRAM and SRAM) can be integrated with CMOS logic circuits (microprocessor) on the same chip because the new device structures, interconnect methods and process technology satisfy both the requirement of high density for memory arrays and the requirement of high performance for logic circuits simultaneously. It is revolutionary that the advent of a new class of merged memory/logic devices can search for information in parallel much more efficiently than today. Second, it overcomes the drawback of the design "bottle neck" (or the von Neumann architecture). Third, it is generally conceded that computers 1000 times faster than today's supercomputers will be required in the future to process image and other array signals in the coming decades. This has led computer scientists to direct their effects toward the area of large-scale multiprocessor networks in which speed is gained through massive parallel arrays of processors. However, clock speeds and data rates are often set by the requirements of off-chip communications. Using the second invention, the functions of hundreds of microprocessor and memory chips can be integrated into a single chip because the proposed device structures and interconnect methods lead to the highest density

integrated circuits in the world. This would eliminate inter-chip communications that require driving long transmission lines between chips. Therefore, the speed of the "massively parallel" laptop supercomputer will exceed that of any other proposed computer in the world.

The fourth great advantage of the second invention is that both memory circuits and logic circuits may achieve ultra density. For example, the layout area of a new full adder is about 8 times smaller than that of a conventional full adder with the same design rules.

BRIEF SUMMARY OF THE INVENTION

It is the principal object of this invention to fabricate ultra dense integrated circuits including dynamic random access memory (DRAM) arrays, static random access memory (SRAM) arrays, and logic circuits using new semiconductor device structures, interconnect methods and fabrication techniques. This is a key to how gate electrode material can be patterned intelligently to achieve ultra dense integrated circuits. Using buried gate structure is another reason to achieve ultra dense integrated circuits. The Buried Gate Transistor (BGT) has less short channel effect, higher reliability and reproducicitivity, and better device uniformity than any other vertical transistor; the BGT has higher performance (or higher current drivability) and higher density than any advanced planar transistor because the BGT has a larger effective channel width, even in a small occupied area. Second, the problem of limitation in the channel length imposed by lithography is overcome. Third, the BGT has higher immunity against misregistration and higher yield than any conventional device. Therefore, the BGT is superior to any other transistor in the world.

An important improvement of this invention is that bit lines of an ultra dense dynamic random access memory array are below all transistors including access transistors and logic transistors and storage capacitors are above all the transistors. This eliminates trench-to-trench punch through leakage current because storage nodes are completely surrounded by insulators. The storage nodes are made up of multiple level interconnects. This reduces the complexity and difficulty of fabrication process and the surface irregularity. Said new cell is named Buried Bit Line (BBL) cell.

Since the spacing between two neighboring storage nodes in the BBL array is much smaller than a minimum lithographic line width, the storage nodes occupy almost all the area of said DRAM array. This makes the size of trench capacitors achieve a maximum limit at a given trench height (or depth). Large capacitor and small leakage current lead to high soft-error resistance.

The BBL array with a minimum of 4 lithographic squares cell size can be integrated on the same chip with ultra dense full single crystal silicon 6-T static random access memory array with a minimum of 40 lithographic squares cell size and extremely high density logic circuits. Access transistors of said DRAM, driving, load and access transistors of said SRAM, periphery CMOS transistors and CMOS logic transistors are BGTs and can be integrated on a single chip with the same gate and channel lengths. However, any conventional vertical transistors cannot accomplish this because they cannot simultaneously satisfy all the requirements of different kinds of devices.

During the fabrication process of ultra dense integrated circuits (Figs. 7A-7H10), since selective etching, doping effect of etching, sidewall spacers 80, and protective layers 63 and 64 of

a conductive layer 62 are used, and since an interconnect layer 75 and a cell plate 221 are patterned at the same time, 14 mask levels are completely saved for said vertical transistor integrated circuits. This reduces the complexity of the fabrication process for vertical devices and solves the wiring problem, and the difficulty in forming interconnects between vertical transistors. The new process shown in Figs. 7A-7H10 is also more simple than the advanced planar device processes.

DESCRIPTION OF THE PREFERRED EMBODIMENT

In the following description and as shown in Figs. 1A through 15C, specific P and N conductivity type materials and regions are indicated. These indications are by way of example and shall not be deemed to limit the teachings of the present invention. It will be understood that devices having opposite P and N arrangements are considered equivalent in all pertinent respects to the devices described herein.

Embodiment 1:

Fig. 1I6 includes a plane view of one kind of 4-F cell according to an embodiment of the

present invention and a section view along line 1I6.

In the drawings, reference numeral 1 denotes a p-type silicon substrate, 2 denotes an N^+-type storage node, 3 denotes a p-type body region, 97 denotes a p-type channel region, 18 denotes a lightly p-doped body region, 55 denotes a shallow and lightly n-doped source or drain extension region, 4 denotes a n-type source or drain, 5 denotes an N^+-type source or drain, 6 denotes a polycrystalline silicon layer (plate), 7 denotes dielectrics for capacitors, 8 denotes gate dielectrics, 9 denotes a gate electrode or a word line, 29 denotes a part of word line, 11 denotes a passivation layer (dielectrics), and 12 denotes a bit line (metal).

In the embodiments of Figs. 1A-15C, the portions designated by the same reference numbers are the same or equivalent portions to those of Fig. 1I6, and are not explained unless they are modified.

Figs. 1A-1I11 are plane and section views illustrating the steps in a process for producing memory cells according to Embodiment 1 of the present invention. The process consists of the following steps:

(1) A heavily n-type doped layer 2 and a very lightly p-type doped layer 18 are first formed respectively by the in-situ doping epitaxy method on a heavily p-doped silicon substrate 1 (Fig. 1A). Then layers 3, 4 and 5 are formed respectively by ion-implantation (Fig. 1B). Choosing ion-implantation to form regions 3, 4 and 5 is due to the implantation process providing high uniformity and precise control over ion energy and dose. Figs. 1A-1B also show the preferred dopant concentrations in layers 1,2, 18, 3, 4 and 5.

(2) Dielectric (Si_3N_4 or SiO_2) 27 is deposited on the layer 5 and then patterned as a trench etching mask. The relative shallow trenches are engraved by anisotropic etching. After the etching, dielectric (Si_3N_4 or SiO_2) sidewall spacers 16 are formed by anisotropic RIE etching (or plasma etching) in a well-known way (Fig.1C). If the dielectric 27 is Si_3N_4, the sidewall spacers 16 are SiO_2. It means that the dielectric 27 and the sidewall spacers 16 are made of different kinds of dielectric materials. The sidewall spacers 16 can be selectively removed while the dielectric 27 remains on the layer 5. For example, a buffered HF solution can offer high SiO_2/(Si_3N_4 and Si) etch selectivity. Si_3N_4 can be selectively removed using silicon nitride etching solution, such as phosphoric acid, U.S. patent No. 3,859,222 or Transetch-N which the Transene Company Inc. has developed and sells commercially. (Transetch-N selectively etches Si_3N_4 in the presence of SiO_2 or Si. It contains no fluoride, produces no undercutting, provides a wide margin of safety in selection of etching times.) The sidewall spacers 16 not only increase the perimeter of the silicon

pillar to achieve large occupied areas of the capacitor, but also protect the channel region of devices from the second relative deep trench etching. Therefore, the channel regions are less damaged by RIE (or plasma etching). The second relative deep trenches are engraved into the heavily p-doped substrate 1. This improves device isolation and suppresses cell leakage current. It is well known that either chlorine or bromine may be used as carrier gases for said two anisotropic trench etching. Bromine is preferred because it offers higher Si/SiO_2 etch selectivity (It is cited from IEDM 91, p. 836 and Manos and Flamm, "Plasma etching an introduction", pp. 146-148.). The sidewall profile of high aspect-ratio trenches is made almost vertical. After the second trench etching, all the exposed silicon surfaces are cleaned by slightly etching the surfaces using HNO_3(60%)-HF(<0.2%)-H_2O solution with an extremely low HF concentration. The method removes near-surface damage and reduces the concentration of heavy metal surface impurities to one tenth that of RCA cleaning. The slight etch method is used for pre-oxidation cleaning of silicon trenches formed by reactive ion etching. MOS c-t retention time and defect density of thermal SiO_2 in trench capacitors is significantly improved by the cleaning. The slight etch cleaning technique yields ultra clean and damage-free surfaces, and significantly improves MOS device characteristics (It is cited from IEDM 88, p.726). After the cleaning, dielectrics 7 for capacitors are formed by thermal oxidation or are deposited on the surface of the trenches to form a capacitor. The dielectrics for capacitors 7 may be silicon oxide films, silicon nitride films, or multi-layer films consisting of silicon oxide films and silicon nitride films (e.g., SiO_2/Si_3N_4 or $SiO_2/Si_3N_4/SiO_2$), or high dielectric constant insulator films (e.g., Ta_2O_5 or $Ba_{0.5}Sr_{0.5}TiO_3$). The oxide/nitride/oxide is preferred here as the capacitor dielectric because of its excellent reliability. The ONO is formed using the conventional method of growing thermal oxide to form the first thin oxide, and partially reoxidizing the silicon nitride to form the top oxide. Thereafter, so the capacitor plate will form, the n-type or p-type polycrystalline silicon 6 is deposited and etch-backed (Fig. 1D). For the high aspect ratio trenches, the polycrystalline silicon 6 is replaced by amorphous silicon to minimize voids. When high aspect ratio trenches are filled with regular polysilicon, voids are formed, which is a reliability concern. There are several reasons for the void formation. Because of the high aspect ratio of the trench, the polysilicon deposition rate is slightly higher near the top of the trench than it is near the bottom. As a result, during the poly fill, the top portion of trench tends to close sooner than the bottom, leading to the formation of voids. In addition, if the polysilicon grain size is comparable to the trench dimension, a nucleated grain may inhibit the filling below it, also leading to void formation. Amorphous silicon minimizes void formation. Amorphous silicon is meta-stable, and recrystalization to regular polysilicon is triggered by any heat cycles after the deposition.

(3) The dielectric spacers 16 are selectively removed by wet etching, followed by an important process step. Slightly oblique rotating ion-implantation is used to implant n-type dopants to adjust

threshold voltage and form shallow source/drain extension regions 55 for vertical MOSFETs (Fig.1E). The process step leads to low threshold voltage in the channel regions 97 and high punch-through resistance in the body region 3 because p-type dopant concentration is partly compensated by the implanted n-type dopants to reduce effective p-type dopant concentration in the channel region. Shallow source/drain junctions will also further prevent punch-through phenomenon and reduce short-channel effects. Since the direction of ion-implantation is almost vertical to source/drain junction depth, more shallow source/drain junction can easily be achieved than conventional ion implantation whose direction is almost parallel to source/drain junction depth. Due to very lightly doped body regions 18, the source/body and drain/body parasitic capacitance is reduced. Fig.1E1 shows the dopant concentrations of different regions of the device.

(4) The gate oxide 8 is formed on the whole surface at 800 °C in the dry oxygen with HCl or H_2O_2. Before the formation of the gate oxide 8, all the exposed silicon surfaces are cleaned by slightly etching the surfaces using HNO_3(60%)-HF(<0.2%)-H_2O solution with an extremely low HF concentration. The gate oxide 8 may, of course, be formed before slightly oblique rotating ion-implantation. After the formation of gate oxide 8, a heavily n-doped polysilicon film 9 is deposited on the whole surface as a material to form a gate electrode or a word line. The polysilicon may, of course, be replaced by a silicide or metal such as WSi_2, $MoSi_2$, $TiSi_2$, W or Al, or by a multi-layer structure, i.e., a polycide structure consisting of such a silicide and polysilicon. The polysilicon 9 thereafter is patterned to form the gate electrodes and word lines. This is a key to how the film 9 can smartly be patterned to achieve an extremely small cell size of a minimum of 4 lithographic squares. Several methods are proposed in the present invention.

(a) Metal 29 is deposited by CVD all over the wafer and then etch-backed to expose the portion of polysilicon over the top part of the silicon pillar islands (Fig. 1F). Thereafter, as shown in Fig. 1G, the metal 29 is patterned by selectively anisotropic plasma etching with the second mask. Selective etching ensures that the polysilicon 9 is not etched or is slightly etched. Metal 29 may, of course, be replaced by any conducting material which can be selectively etched on the gate material 9. Figs. 1G1-1G2 are section views along the lines 1G1 and 1G2 of the same structure in Fig. 1G. In spite of nearly 50% misregistration, which is unacceptable in a conventional cell, the new cell is not degraded. From different cross sections and positions, figs. 1G3-1G4 show that the new cells have high immunity against misregistration. After the metal 29 is patterned, the exposed polysilicon 9 is etched by selectively anisotropic plasma etching using CF_4+O_2, CF_4+N_2, $CClF_3$, Cl_2+O_2, NF_3/HCl, $HBr+Cl_2+SF_6$, $Cl_2+BCl_3+He+O_2$, $SiCl_4+Cl_2+BCl_3+He+O_2$, chlorine or bromine as an etchant gas in a familiar way. The portion of polysilicon over the top part of the silicon pillar islands and the exposed bottom portion of polysilicon are completely removed by said plasma etching; on the other hand, the part of the polysilicon along the sidewalls of the silicon

islands remains,because the height of the sidewall polysilicon is higher than the thickness of the polysilicon film 9. The remaining polysilicon is lower than the dielectric 27 and the silicon pillar island because the polysilicon 9 can be etched with a selectivity which favors the dielectric 27. This is very important for the new cell structure. The portion of polysilicon under the metal 29 is not etched due to protection of the metal 29. So the remaining sidewall polysilicon, the portion of polysilicon under the metal 29 and the metal 29 form gate electrodes and word lines (Figs. 1H-1H2). The metal 29 is not only the patterning polysilicon 9 mask but also part of the word lines. This reduces the resistance of the word lines. Figs. 1H3-1H4 show that the patterning word line process step has high immunity against misregistration. All kinds of the proposed cells or devices in the present invention have this advantage, so I need not mention this advantage in the following sections again.

b) From Figs. 1H1-1H2 and 1H4, we can see that a polysilicon cell plate 6 is etched during the etching of polysilicon 9. In order that a cell plate 6 not be etched or only slightly etched, another method should be used. The metal 29 is deposited by CVD all over the wafer and then etch-backed to expose the portion of polysilicon over the top part of the silicon pillar islands (Fig. 1JA). Thereafter, as shown in Fig. 1JB, the polysilicon 9 and the metal 29 are etched to the proper height without a mask, and afterwards, the metal 29 is patterned by selectively anisotropic plasma etching with the second mask (Fig. 1JC). After the metal 29 is patterned, the exposed polysilicon 9 is etched by plasma etching. The exposed bottom portion of polysilicon is completely removed by said plasma etching. So the remaining sidewall polysilicon, the portion of polysilicon under the metal 29 and the metal 29 form gate electrodes and word lines (Fig. 1JD).

c) The metal 29 as a patterning mask of the polysilicon 9, of course, may be replaced by photoresist or dielectric (SiO_2 or Si_3N_4) 20. The photoresist or dielectric 20 is deposited all over the wafer and then etch-backed to expose the portion of polysilicon over the top part of the silicon pillar islands (Fig. 2B). Thereafter, as shown in Fig. 2CA, the polysilicon 9 is selectively etched to the proper height without a mask. Then the photoresist or dielectric 20 is patterned by selectively anisotropic etching with the second mask (Fig. 2CB). For example, SiO_2 can be etched selectively and anisotropically using CF_4/H_2, HF, HBr, or CHF_3 as an etchant gas by familiar means. Si and Si_3N_4 are not etched or are only slightly etched by the selective etching. For example, CHF_3 gas gives an etch rate ratio of SiO_2 to Si of about 10. Si_3N_4 can be etched anisotropically in the RIE mode with a selectivity to Si and SiO_2 of 20. Either of two source gases, CH_2F_2 or CH_3F, can produce these results. After the photoresist or dielectric 20 is patterned, the exposed polysilicon 9 is etched by plasma etching. The exposed bottom portion of polysilicon is completely removed by said plasma etching, so as a result, the remaining sidewall polysilicon and the portion of polysilicon under the metal 29 form gate electrodes and word lines. After the formation of word

lines, the photoresist 20 must be removed (Fig. 2CC). If the dielectric 20 is the patterning mask of polysilicon 9, it is not necessary to remove dielectric 20. In this method, the cell plate 6 is not etched.

d) The photoresist or dielectric 20 is deposited all over the wafer and then etch-backed to expose the portion of polysilicon over the top part of the silicon pillar islands (Fig. 2B). Thereafter, the photoresist or dielectric 20 is patterned by selectively anisotropic etching with the second mask. Then the exposed polysilicon 9 is etched by plasma etching. The exposed bottom portion of polysilicon is completely removed by said plasma etching. So the remaining sidewall polysilicon and the portion of polysilicon under the metal 29 form gate electrodes and word lines (Fig. 2C). In this method, a part of the cell plate 6 may be etched.

The above proposed methods have one point in common in so far that both of the portions of polysilicon over the top part of the silicon pillar islands and the upper portion of polysilicon along the sidewalls of the silicon islands are completely removed while both the portion of polysilicon on the cell plate 6 in some places and the lower portion of polysilicon along the sidewalls of the silicon island remain. The goal in mind is to use certain materials to protect the bottom portion of polysilicon while leaving unprotected the upper portions of polysilicon.

(5) After the formation of gate electrodes and word lines, a thick dielectric (SiO_2) 11 is deposited by CVD. After the thick CVD deposit has been produced, a thick photoresist is deposited. The photoresist is usually so thick that it covers all the steps well, making the top surface flat. A plasma or reactive-ion-etching process is chosen to etch the resist and the CVD deposit at the same rate. The surface is etched until all resist and part of the deposit is etched off, leaving the surface flat (It is cited from S.M. Sze, "VLSI Technology", 1988, p. 415). The RIE etch back is followed by chemical mechanical polish (CMP) to improve the result of planarization further. The feature of the CMP is that the removed rate of the small elevated features (spikes) is larger than the averaging effect of the removal rate over all the exposed regions (See IEDM 89, p. 61). CMP can provide global thickness uniformity of 10% over the wafer (See IBM J. Res. Develop., Vol. 34, No.6, Nov. 1990, p. 864).

(6) After the planarization process, the dielectric (SiO_2) 11 is etched to a proper depth by using selectively anisotropic plasma etching with the third mask. The silicon region 5 is not etched or is only slightly etched. Thereafter, metal (or polysilicon, polycide) 12 is deposited and etched back to remove excess metal 12 on the upper surface of the dielectric 11 to form the bit lines. The method of formation of bit lines and bit line contacts used here save a mask level. For conventional methods, the formation of bit line contact holes and the formation of bit lines each need a mask

level. From different direction, fig. 1I1 gives a cross section view along the line 1I1 of the same structure in Fig. 1I. Even if close to 50% misregistration occurs, unacceptable in a conventional cell, the new cell is not influenced because the sidewall bit line contact is used (Fig.1I2). Since the gate electrodes 9 is much lower than the vertical position of the bit line and top part of n-doped source or drain regions 5, top and side bit line contact can be used to reduce the contact resistance and eliminate the registration tolerances of the contact hole. In other words, the position of gate electrodes 9 is low enough that the bit line contacts (or bit lines) and word lines (or gate electrodes) can not short-circuit even if they are at the same horizontal position. The new access transistor of DRAM cell is named buried gate transistor (BGT). In the conventional SGT cell (surrounding gate transistor cell developed by K. Sunouchi *et al.*), the intended gate length equals the height of the first trench (or the height of the upper portion of the pillar silicon island). The result is that the gate electrode has the same vertical position as the bit line contact. In order to avoid short-circuiting of the word line and bit line contact, the size of the pillar silicon island must be much larger than 1 minimum lithographic square. The new cell in the present invention not only can eliminate the registration tolerances of the contact hole but also can achieve a relatively high yield since it is permissible that the worst-case misregistration distance for all the masks equals ~ 50% of minimum feature. The buried gate structure is another reason that it is desirable to achieve an extremely small cell size of a minimum of 4 lithographic squares. From different positions, figs. 1I3-1I5 give different cross section views along the lines 1I3, 1I4 and 1I5 respectively of the same structure in Fig. 1I2. Figs. 1I6-1I11 show that the proposed cells have high immunity against misregistration for all the mask levels. Figs. 1I6-1I11 show the same structure along the different lines. All varieties of the new cells or devices in the present invention have this advantage.

In order to reduce the parasitic capacitance of the word lines 9 and the cell plate 6, the relative thick dielectric (SiO_2) 8 is formed between the word lines 9 and the cell plate 6 (Fig. 1K). The dielectric (SiO_2) 8 is formed with the gate oxide 8, simultaneously using the method of concentration-enhanced oxidation. This will not increase the complexity of the process. This oxidation process will grow a relatively thick layer of oxide on the surface of the highly n-doped polysilicon cell plate 6 and a thinner layer of oxide on a lightly doped silicon surface. It is well known that the higher the dopant concentration and the lower the temperature are, the result of concentration-enhanced oxidation is more obvious. The ratio of the thickness of the dielectric on the cell plate 6 and the thickness of the gate oxide can be well controlled by the dopant concentration and temperature.

Embodiment 1 (Figs. 1A-1K) has the following major advantages over conventional device structures and fabrication processes.

1) An ultra dense dynamic random access memory (DRAM) array with a minimum of 4 lithographic squares cell size can be achieved by the new cell structure and fabrication process, so the cell is named 4-F (feature size) cell.

2) The metal 29 is not only a patterning polysilicon 9 mask but also a part of word line (or interconnect between the gate electrodes) to reduce the resistance of word line.

3) The 4-F cell can increase the soft error resistance against alpha particles to prevent the flow of leakage current among the cells. It is well known that soft error resistance is increased by reducing the diagonal length of the depletion region in the memory cell. This suggests that higher density cell structure leads to higher soft error resistance. Second, the collection efficiency and the generation of electron-hole pairs induced by alpha particles are dependent on the impurity concentration and its profile, thus the high doped substrate 1 and storage node 2 increase the soft error resistance.

4) It is well known that actual storage capacitance depends on trench sidewall doping concentrations in a conventional trench cell. A higher doping concentration provides a larger capacitance, thus the high doped storage node 2 provides a larger storage capacitance than available in the conventional cell. Secondarily, the high doped storage node 2 reduces source/drain parasitic resistance.

5) In order to reduce the DRAM cell area, a vertical access device has been used in a trench-transistor cell and a surrounding gate transistor cell. However, a vertical access transistor suffers from non-uniformity and low performance. For example, the channel length of SGT (developed by K. Sunouchi *et al.*) is determined by the height of the first trench. However, uniformity of the channel length is difficult to control because of the non-uniform nature of the plasma etch process. Second, the threshold voltage adjustment is achieved only by the well impurity concentration. However, the channel length and threshold voltage of BGT are determined by ion-implantation. The implantation process provides high reproductivity and uniformity. The advantages of using ion implantation are precise control over impurity dose, depth, profile and area uniformity, thus the BGT has better device uniformity. It is compatible to the planar transistor technology that threshold control of BGT can be achieved by ion-implantation.

6) Since the channel length of BGT is determined by ion implantation, the problem of limitation in the channel length imposed by lithography is overcome, thus sub-half micro MOSFETs can be fabricated using conventional optical lithographical techniques to achieve high speed and high current drivability. If the BGT uses conventional vertical sandwich structures (for example, vertical

IGFETs, VMOS, UMOS and SGT), it suffers from poor reliability and short channel effects including the geometry effects, punch-through phenomenon and turn-off behavior due to large S/D junction depth. Because the source, channel (or body) and drain regions are in an overlapping relationship to one another, the source-channel and drain-channel junctions are the whole size of a pillar silicon island. In order to reduce S/D junction depth for vertical FET, a shallow and lightly n-doped source or drain extension region 55 are formed in the proposed device. The said region surrounds the inner periphery of a pillar silicon island. Second, any conventional vertical transistor suffers from large source-channel (or body) and drain-channel (or body) parasitic p-n junction capacitances, which are inherent to vertical sandwiched structures. However, the existence of a very lightly p-doped body region 18 in BGT reduces the total S/D parasitic p-n junction capacitances to improve the device speed because the dopant concentration of the body region 18 is much lower than that of the body region 3.

7) The BGT can use the most advanced planar transistor structures, such as fully overlapped LDD (FOLD) MOSFETs, source-to-drain non-uniformly doped channel (NUDC) MOSFETs, and double lightly doped drain (DLDD) MOSFETs (Figs. 1I6 and 5E1). A number of planar FOLD MOSFETs have been fabricated and characterized. It has been proven that the FOLD device improves device performance and reliability compared with conventional LDD and single drain device. Although the FOLD device increases the gate-source/drain overlap capacitance, the increase of the current drive through S/D resistance reduction is important in dense circuits, where wiring capacitance is significant. Therefore, BGT with the FOLD structure is suitable for high performance, high reliability sub-half micron device application.

In conclusion, the BGT has less short channel effect, higher reliability and reproducibility, and better device uniformity than any other vertical transistor; the BGT has higher performance (or higher current drivability) and higher density than any advanced planar transistor because the BGT has a larger effective channel width even in a small occupied area. Secondly, the problem of limitation in the channel length imposed by lithography is overcome. So the BGT is superior to any other transistor in the world. The 4-F cell have smaller cell size, higher soft error resistance, higher storage capacitance, higher immunity against misregistration and higher yield than any conventional cell.

The above presented vertical device structures are body-float, which are similar to SOI MOSFETs. Some people think that floating-body SOI MOSFETs suffer from parasitic bipolar junction transistor-induced breakdown and latch phenomena, which result in large power-consumption in SOI-CMOS. However, since power supply voltages are constantly being reduced with down-scaling of device, body-float device will not consume much power because parasitic

bipolar junction transistor effect will not exist if operation voltage is below 3.3 volts. The breakdown voltage of SOI MOSFETs is usually above 6 volts, so this breakdown voltage is high enough for device operation. Third, the latch phenomena, which occurs at high drain biases (~5 volts), is an extreme case of floating-body effects. However, it is generally conceded that device operation voltage must be below 3 volts for 256 Mbit integrated circuits, so the floating-body effects cannot influence the body-float devices.

Any similar structure feature, process and advantage will not be described again or will be only lightly mentioned in the following sessions.

Embodiment 2:

Figs. 2A-2D are plane and section views illustrating the steps in a process for producing floating-body free memory cells. The process consists of the following steps:

(1) The very lightly doped P− layer 18 is first formed by the in-situ doping epitaxy method on a heavily p-doped silicon substrate 1. Thereafter the dielectric (Si_3N_4 or SiO_2) 27 is deposited on the layer 18 and then patterned as trench etching mask. The relative deep trenches are engraved into the heavily p-doped silicon substrate 1 by anisotropic trench etching. Slightly oblique rotating ion-implantation is used to implant n-type dopants into silicon pillar islands to form the shallow regions 19 (Fig. 2A). The concentration of the implanted n-type dopants is higher than the concentration of p-type dopants in the region 18, but lower than the concentration of p-type dopant in the substrate 1.

(2) After the trench etching, all the exposed silicon surfaces are cleaned and the dielectrics 7 for storage capacitors are formed. Thereafter, the n-type polysilicon or amorphous silicon 6 is filled in the trenches to form the plate of the capacitors. Then the gate insulator 8 is formed and the polysilicon 9 is patterned to form the gate electrodes and word lines (Figs. 2B, 2C, 2CA, 2CB and 2CC).

(3) The dielectric 27 is selectively removed (This step is not necessary.), followed by three ion implants. The ion implants form the p-doped channel (or body) regions 3, the lightly n-doped source (or drain) regions 4 and the heavily n-doped source (or drain) regions (or ohmic contact regions) 5. The channel (or body) dopant concentration is well controlled by the first ion implant. The concentration of p-dopant in the first ion implant is higher than the concentration of n-type dopant in the region 19. The channel length is exactly determined by the first two ion implants (Fig. 2D). If the doping profile of the first ion implant is used intelligently, the channel length can be determined by the first ion implant (Fig. 3) alone. Fig. 3 shows a preferred channel doping

(4) All the exposed silicon surfaces are cleaned after the trench etching is accomplished, and afterwards the dielectrics 7 for storage capacitors are formed. Thereafter, the n-type doped polysilicon or amorphous silicon 6 fills the trenches in order that the plate of the capacitors will form. The Si_3N_4 17 is deposited by plasma-enhanced CVD (PECVD) and etched back, using CH_2F_2 or CH_3F as an etchant gas in a familiar way (Fig. 5D). The silicon region 22 and SiO_2 sidewall spacers 21 are hardly etched because CH_2F_2 or CH_3F can achieve a high Si_3N_4 : Si and Si_3N_4 : SiO_2 etch rate ratio of about 20 : 1. The Si_3N_4 17 can reduce the parasitic capacitance between the word line 9 and the cell plate 6.

(5) The SiO_2 spacers 21 are selectively removed by wet etching, and afterwards all the exposed silicon surfaces are cleaned. Thereafter the gate insulator 8 is formed and the polysilicon 9 is patterned to form the gate electrodes and word lines, followed by multiple ion implants. The multiple ion implants form source-to-drain non-uniformly p-type doped channel (or body) regions 31, 32 and 33, the lightly n-doped source (or drain) region 4 and the heavily n-doped source (or drain) region 5. The nonuniform regions 31, 32 and 33 may be formed by the first three ion implants or may be formed by only one implant, using the doping profile of implantation. Fig. 5E shows a source-to-drain non-uniformly doped channel (NUDC) structure of the BGT. It is proven that the mobility of the NUDC MOSFET is increased as compared with that of the conventional channel MOSFET, and also, the V_{th} lowering of the NUDC MOSFET is suppressed as compared with that of the conventional channel MOSFET. For the vertical NUDC BGT, the non-uniform impurity profile in the channel region can be in-situ doped or easily and precisely controlled by conventional implantation . In general, non-uniforml doping in the channel adds a new freedom in device design. If the dopant concentrations of the regions 32 and 33 are lower than that of the region 31, the structure shown in Fig. 5E is a double-lightly doped drain MOSFET. It is found that the DLDD MOSFET is one of the most promising device structures for sub-half micron MOSFETs which can operate at 5 volts of supply voltages. This structure has an impurity profile of N^+-N^--P^--P-P^--N^--N^+ along the surface of the silicon pillar island. It is clear that the DLDD MOSFET has excellent characteristics, such as high drain sustaining voltage, less short channel effect, high current drivability and high reliability. After the multiple ion implants, the dielectric 11 is deposited by CVD and planarized, and finally, the bit lines 12 are formed. The multiple ion implants may, of course, be used before the SiO_2 spacers 21 are selectively removed, before the gate electrodes are formed, or after the dielectric 11 is planarized. Fig. 5E1 shows that the cells shown in Fig. 5E have high immunity against misregistration. Fig. 5E2 gives a different section view along the line 5E2 of the same structure shown in Fig. 5E1.

The new device structures and methods of fabrication not only can form an ultra dense dynamic

random access memory (DRAM) array with a minimum of 4 lithographic squares cell size, but also can achieve much higher density logic circuits than any other conventional logic circuits.

Embodiment 3:

Figs. 6A-6K are plane and section views, illustrating the steps in a process for integrating logic circuits with memory arrays. Although there are a plurality logic circuit types, all the logic circuits have a similar method of fabrication. The full adder is chosen as an example of logic circuits since it is the fundamental unit of the arithmetic operations and it forms important components in a plurality of systems. The process consists of the following steps:

(1) A very lightly p-type doped layer 206 is first formed by the in-situ doping epitaxy method on a heavily p-doped silicon substrate 1. Afterwards, a oxide layer 220 is formed on the layer 206 by thermal oxidation or CVD. Thereafter, photoresist 200 is deposited and patterned as the first mask, followed by ion implantation. N-type dopants (e.g., P^+, As^+ or Sb^+) are implanted to form heavily n-doped regions 201. A oxide film 202 is selectively deposited, using LPD (liquid phase oxide deposition) technology without stripping the photoresist 200 (Fig. 6A). The selective deposition occurs at room temperature and only at the oxide surface (cited from IEDM 91, p. 637.). The photoresist is stripped after the oxide deposition, then triple implants are performed. The first implant with high ion energy is used for formation of the heavily n-type doped region 203, the second implant with medium ion energy for formation of the lightly n-type doped region 204, and the third implant with low energy for formation of the heavily p-type doped region 205 (Fig. 6B). Recently, Mitsubishi Electric Corporation reported that a heavily doped buried layer could be formed without increasing leakage current if self-gettering or proximity gettering of the secondary defeats induced by high energy ion implantation was utilized. Second, since the ion implants which form the regions 201, 203, 204 and 205 do not go through the channel region of devices, the crystalline quality of these layers is less important. In this process, the regions 201, 203, 204 and 205 are formed with only one mask. Said regions may, of course, be formed with two masks, but this creates the registration tolerances that reduce the device density. The LPD oxide film 202 does not need to be very thick. Even if the implanted ions with high energy go through the LPD oxide film 202, they are placed into the regions 201 rather than the regions 206.

(2) Undoped silicon layer 152 is epitaxied on the regions 201 and 205, and afterwards, Si_3N_4 27 is deposited on the layer 152. The Si_3N_4 and undoped silicon layer 152 are patterned with the second mask. After the patterning, thin SiO_2 layer 21 is grown on the silicon surface by thermal oxidation. The SiO_2 sidewall spacers 21 are formed by selectively anisotropic etching (Fig. 6C).

(3) The different deep trenches are engraved into the regions 201, 204, 205 and 206 by plasma

etching with the third mask. The formation of the different deep trenches with only one mask and one time etching is due to the use of the doping effect of etching. If the trenches are formed by Cl atom plasma etching using such as Cl_2, Cl_2+Ar, CCl_4+Ar, CF_3Cl, $SiCl_4+O_2$, CF_3Br+Cl_2 or $C_2F_6+Cl_2$ as an etchant gas, the etching rate of the heavily n-doped region 201 is 15-25 times larger than that of the undoped or lightly doped regions 204 and 206, while the heavily p-type dopants in the region 205 suppress silicon etch rates by as much as a factor of slightly less than two. The doping effect in F atom plasmas is less than that in Cl atom plasmas (Manos and Flamm, "Plasma etching an introduction", pp. 148-149), so it is preferred that the different deep trenches be formed by Cl atom plasma etching to save a mask level. After the trench etching, all the exposed silicon surfaces are cleaned, and a very thin SiO_2 film is grown on the silicon surface. This thin SiO_2 film is good for reducing the leakage current, as a means to improve the device isolation. After the thin SiO_2 film is grown, thick SiO_2 207 is deposited by PECVD and then planarized and etched back by selectively anisotropic etching to fill the trenches (Fig. 6D). The heavily n-doped buried layer 203 and the heavily p-doped substrate 1 are used to reduce alpha-particle-induced soft errors. The combination of the different deep trenches, the heavily n-doped buried layer 203 and heavily p-doped substrate 1, improves device isolation and completely eliminates latchup in CMOS. The reason why CMOS has latchup effect is that the base-emitter junctions for parasitic NPN and PNP bipolar transistors in CMOS are sufficiently forward-biased (V_{BE} = 0.7 volts) to provide significant leakage current. The fact that 0.7 volts forward bias is produced in the conventional device structures is due to the relatively large resistances associated with the well and the substrate. In the new device structure, the heavily n-doped buried layer 203 and heavily p-doped substrate 1 are base regions of parasitic PNP and NPN bipolar transistors, respectively, thus 0.7 volts forward bias can not exist. Second, the heavily n-doped buried layer 203 and heavily p-doped substrate 1 can greatly reduce the common-emitter current gains for both PNP and NPN bipolar transistors. Therefore, latchup in CMOS should be completely eliminated in the novel device structure.

(4) The Si_3N_4 27 and SiO_2 sidewall spacers 21 are selectively removed. N-type and p-type dopants are implanted respectively using different ion energies and doses with the fourth mask to form NMOS relative low p-doped body regions 32, relative high p-doped body region 3, lightly n-doped source or drain regions 4 and heavily n-doped source or drain regions 5. A slightly oblique rotating implantation is used to implant n-type dopants to form low threshold voltage channel region 97 and shallow source/drain extension regions 55. After the channel, body, source and drain regions of NMOS are formed, PMOS relative low n-doped body regions 33, relative high p-doped body region 48, lightly p-doped source or drain regions 50, heavily n-doped source or drain regions 51, buried-channel region 49 and shallow source/drain extension regions 57 are formed by a similar method with the fifth mask. Since the direction of ion-implantation is almost parallel to the

channel direction, thinner buried p-doped layer 49 can be formed to improve subthreshold characteristics of buried-channel PMOS. More shallow source/drain extension regions 57 can be also formed at the same time to reduce short channel effects and increase punch-through resistance. In the novel device structure, the region 3 determines the punch-through resistance of NMOS, the regions 32 reduce source/body and drain/body parasitic capacitance of NMOS and the region 97 determines threshold voltage of NMOS; the region 48 determines the punch-through resistance of PMOS, the regions 33 reduce source/body and drain/body parasitic capacitance of PMOS and the region 49 determines threshold voltage of PMOS. The threshold voltage of the vertical MOSFETs is determined not only by ion implantation dosage and energy but also by ion implantation angle. After the ion implantation process, all the exposed silicon surfaces are cleaned. Low thermal budget gate insulator 8 is formed to minimize redistribution of impurities. The implanted impurities are activated by the thermal cycle during growth of the gate insulator. There are several methods to form low thermal budget gate insulator 8.

(a) An approximately 5 to 10-nm-thick gate oxide 8 is formed with HCl oxidation between 700 - 800 °C after the preoxidation cleaning. Introduction of a low percentage dosage (1 to 9% by volume) of HCl to the oxygen during oxidation improves the film quality, acts as a gettering agent for sodium in the oxide, and improves a variety of other device parameters. Incorporation of HCl during oxidation does increase the oxidation rate by approximately 30 percent, and thereby reduces the oxidation time and redistribution of impurities during oxidation.

(b) Further reduction of the redistribution of impurities is possible when oxidation is carried out under high pressure (greater than 1 atm) because the growth rate increases in direct proportion to the pressure. This can be put to use in growing gate oxide at low temperatures, and over the short term, can prevent significant redistribution of impurities. For example, we consider the use of high-pressure, low-temperature steam oxidation of silicon. At 10 atm pressure and 750 °C, a 30 nm thick oxide can grow in 30 minutes. The time, temperature, and pressure applied are all variables for determining the thickness. Such a technique has been applied to the growth of a thin gate oxide in the process of fabricating MOS dynamic RAMs. Results of 15 nm thick, high-pressure dry oxides grown at 800 °C and 25 atm showed a breakdown field of 13.6 MV/cm, which was about 10% higher than the 1 atm control group. A growth rate of 1 nm /min was obtained for the same temperature and pressure. Boron impurities diffuse only 3.9 nm at 800 °C in 15 minutes. Therefore, said process of low temperature gate insulator formation does not change the dopant profile. This process can achieve excellent device characteristics.

(c) The gate oxide 8 is also grown on the rapid thermal oxidation systems in a few seconds. Impurities do not have enough time to diffuse.

(d) A thermal/CVD stacked gate insulator may be used. The thermal/CVD stacked gate insulator, in comparison with conventional thermal gate oxide, dramatically reduces the process-induced device degradation responsible for threshold voltage scatter as well as maintaining low defect density and interface state density.

After the gate insulator 8 is formed, the heavily n-doped polysilicon silicon 9 is deposited and patterned with the sixth mask to form the gate electrodes and word lines. Fig. 6E shows a plane and section view of a full adder layout before interconnects between devices are formed. Fig. 6E1 shows a comparison between a planar view of the layout and the full adder circuit. Fig. 6E2 includes a planar view of a DRAM array and a section view along the line 6E2. In order for readers to sufficiently understand the new structure, Fig. 6E3 gives a different section view along the line 6E3 of the same structure shown in Fig. 6E2.

The above proposed PMOS is a buried-channel device with a n-doped polysilicon gate electrode. Both surface channel NMOS and PMOS with dual-polysilicon gates (n-doped and p-doped gates) can be fabricated by the following process. The undoped polysilicon film 9 is first deposited and patterned, followed by ion implantation. The heavily n-doped polysilicon gates and heavily n-doped source/drain regions 5 are formed by ta simultaneous ion implant; the heavily p-doped polysilicon gates and heavily p-doped source/drain regions 51 are formed by another simultaneous ion implant.

(5) After the gate electrodes and word lines are formed, dielectric (SiO_2) 11 is deposited by PECVD and planarized. The dielectric 11 is etched to a proper depth by selectively anisotropic plasma etching with the seventh mask. The silicon regions 5 and 51 are not etched or just slightly etched. Thereafter, polysilicon (single crystal silicon or polycide) 208 is deposited and etched back to remove excess polysilicon 208 on the upper surface of the dielectric 11 to form the first level interconnects (Fig. 6F). Fig. 6F1 gives a different section view along the line 6F1 of the same structure shown in Fig. 6F. In order for observers to see the polysilicon gate electrodes, word lines and other conductive lines, important for understanding the circuit layouts, the dielectric 11 is not shown in the planar views of Figs. 6F and 6F1.

(6) Dielectric (SiO_2) 212 is deposited by PECVD on the polysilicon 208 and planarized, followed by the formation of different deep contact holes. The different deep contact holes are formed by selectively anisotropic etching, using CF_4+H_2, HF, HBr or CHF_3 as an etchant gas with the eighth mask. For example, CHF_3 gas gives an etch rate ratio of SiO_2 to Si of about 10. Therefore, the selectively etching guarantees that only SiO_2 (the dielectrics 11, 207 and 212) is

etched and that the polysilicon 208 and single crystal silicon regions 5, 51, 201 and 205 are not etched, or only slightly etched. The selective etching achieves at least three different deep contact holes: contact holes to the polysilicon 208, contact holes to the single crystal silicon regions 201 and 205, and contact holes to the polysilicon gates or word lines (Figs. 6G, 6G1 and 6G2). This step saves two mask levels for the fabrication of the new device structure. Thereafter, the polysilicon, polycide or metal 209 (e.g., W, Al or Al alloy) is filled into contact holes. Then the second level interconnects 210 (made from polysilicon, polycide or metal) are formed with the ninth mask. Fig. 6G shows the second level interconnects of a full adder circuit. Figs 6G1 and 6G2 give plane and section views of DRAM array along the different lines 6G1 and 6G2 at this stage in the fabrication process. In order for observers to see the polysilicon gate electrodes, word lines, bit lines and polysilicon 208 and other conductive lines, the dielectrics 11 and 212 are not shown in the plane views of Fig. 6G, 6G1 and 6G2. Any dielectric (unconductive material) layer which is above the dielectric 207 is shown in the planar display of the structures. It is not mentioned again in the following sections.

(7) The third level contact holes 230 and interconnects 214 (made from polysilicon, polycide or metal) are formed respectively with the tenth and eleventh masks (Fig. 6H). A full adder has been fabricated at this point in the fabrication process. Fig. 6H1 includes a planar view of DRAM array and a section view along line 6H1 at this point in the fabrication process.

(8) Thereafter, the dielectrics (SiO_2) 212, 213 and 215 on the polysilicon 208 in the area of DRAM array are completely removed by selective etching with the twelfth mask 216. The dielectric (SiO_2) 11 may also be partially etched to a proper depth. Due to the selective etching, the polysilicon 208 is not etched, or only slightly etched(Fig. 6I).

(9) After the dielectrics 212, 213 and 215 are removed, a very thick n-doped polysilicon 218 is deposited all over the wafer, planarized and then etched back. A global thickness uniformity of 10% over the wafer is necessary. Si_3N_4 216 is deposited and patterned with the thirteenth mask afterwards. After this, Si_3N_4 217 is deposited and etched anisotropically to sidewall spacers (Fig. 6J). The distance between two sidewall spacers 217 is much smaller than a minimum lithographic line width. Fig. 6J1 gives a planar view at this stage in the fabrication process.

(10) The polysilicons 218 and 208 are selectively etched using the Si_3N_4 216 and 217 as a mask. Due to the selective etching, the etching stops at dielectric 11. After the etching, the dielectrics (Si_3N_4) 216 and 217 are selectively removed. The dielectrics (SiO_2) 215, 213, 212 and 11 are not etched, due to selective etching. Dielectrics 224 for capacitors are formed. The oxide/nitride/oxide is preferred here as the capacitor dielectric because of its excellent reliability.

Thereafter, for formation of the capacitor plate, the n-type or p-type doped amorphous silicon 221, to fill the very narrow spacings between storage nodes, is deposited and planarized. Amorphous silicon is recrystalized to regular polysilicon by the annealing which follows. Amorphous silicon (or polysilicon) 221 is patterned with the fourteenth mask. Thereafter, dielectric (SiO2) 222 is deposited by PECVD. The first level global metal interconnect contact holes and interconnects 260 are formed with the fifteenth and sixteenth masks (Fig. 6K). The second level global metal interconnect contact holes and interconnects are formed with the seventeenth and eighteenth masks. This step, however, is not diagrammed. The top two level global metal interconnects may, of course, be replaced by the second level interconnects 210 and the third level interconnects 214. The complexity of the entire fabrication process is thereby reduced to fourteen mask levels, and thus there are also no interconnects above the cell plate of the storage capacitors. The storage capacitors may be sufficiently large to satisfy the requirements of different level DRAMs through changing the heights of the polysilicon 208 and dielectrics 212, 213 and 215. The most important characteristics of the new DRAM cell are that the bit lines are below all the transistors (including access transistors and logic transistors) and that the storage capacitors are above all the transistors. The resulting new cell is named buried bit line (BBL) cell. The most serious problem of the trench cell is trench-to-trench punch through leakage current; however, the cell leakage current is dramatically reduced because the dielectrics (or insulators) completely surround the storage nodes of the BBL cells. The size of the BBL cell can be smaller than that of the trench cell and the storage capacitor of the BBL cell can be larger than that of the trench cell because required trench-to-trench spacing in the trench cells is as large as 0.6 μm; on the other hand, required spacing between the storage nodes in the BBL cells can be smaller than 0.1 μm. 6 Reduction of the dopant concentration of the region 206 can greatly reduce the parasitic p-n junction capacitance between the bit line 201 and the region 206.

Figs. 7A-7H10 give an improved structure and process based on the structure and process in Fig. 6A-6K. It is illustrated in Figs. 7A-7H10 that memory circuits (SRAM and DRAM arrays) are integrated with CMOS logic circuits (a full adder, CMOS flip-flop, CMOS NAND and CMOS inverter chain) on a single chip. Inverter, NAND, NOR and transmission gate are the most basic elements in building logic circuits. The NOR structure is not diagrammed, since it is very similar to the NAND structure. The transmission gate is illustrated in the CMOS flip-flop. Both a full adder and a flip-flop are important logic circuits. The fabrication process of the circuits shown in Figs. 7A-7H10 may sufficiently illustrate the fabrication process of all kinds of circuits. The process consists of the following steps:

(1) A very lightly p-type doped layer 206 is first formed by the in-situ doping epitaxy method on a heavily p-doped silicon substrate 1 (Fig. 7A).

(2) Four regions 201, 203, 204 and 205 are formed by triple ion implants with only one mask. Choosing the proper height of the first mask 221 make the dopants with high ion energy in the first implant go through the mask 221 to form the heavily n-doped regions 201. In the exposed silicon areas, the dopants for the first implant go through a certain deep silicon layer to form the heavily n-doped region 203, thus the regions 201 and 203 are formed simultaneously by the first implant. The purpose of the second implant with medium ion energy is formation of the lightly n-type doped region 204, and the purpose of the third implant with low energy is formation of the heavily p-type doped region 205 (Fig. 7B). The dopants with low and medium ion energies cannot go through the mask 221.

(3) Undoped silicon layer 152 is epitaxied on the regions 201 and 205 and thereafter Si_3N_4 27 is deposited on the layer 152. The Si_3N_4 and undoped silicon layer 152 are patterned with the second mask. After the patterning, Thin SiO_2 layer 21 is grown on the silicon surface by thermal oxidation, after the patterning. The SiO_2 sidewall spacers 21 are formed by selectively anisotropic etching. The different deep trenches are engraved with the third mask using the doping effect of etching. After the trench etching, all the exposed silicon surfaces are cleaned, and a very thin SiO_2 film is grown on the silicon surface. Thick SiO_2 207 is deposited by PECVD and then planarized and etched back by selectively anisotropic etching to fill the trenches.The Si_3N_4 27 and SiO_2 sidewall spacers 21 are selectively removed. N-type and p-type dopants are implanted respectively using different ion energies and doses with the fourth mask to form NMOS relative low p-doped body regions 32, relative high p-doped body region 3, lightly n-doped source or drain regions 4 and heavily n-doped source or drain regions 5. A slightly oblique rotating implantation is used for implanting n-type dopants, so that form low threshold voltage channel region 97 and shallow source/drain extension regions 55 will form. After the channel, body, source and drain regions of NMOS are formed, PMOS relative low n-doped body regions 33, relative high p-doped body region 48, lightly p-doped source or drain regions 50, heavily n-doped source or drain regions 51, buried-channel region 49 and shallow source/drain extension regions 57 are formed, using a similar method with the fifth mask. After the ion implantation process, all the exposed silicon surfaces are cleaned. Low thermal budget gate insulator 8 is formed to minimize redistribution of impurities. The implanted impurities are activated by any thermal cycle after the implants. After the gate insulator 8 is formed, the heavily n-doped polysilicon silicon 9 is deposited and patterned with the sixth mask to form the gate electrodes and word lines. Fig. 7C shows a plane and section view of a SRAM array layout before interconnects between devices are formed. Fig. 7C1 shows a comparison between a plane view of the layout of the SRAM array and a SRAM cell circuit. Fig. 7C2 includes a plane view of a full adder and a section view along the line 7C2. Fig. 7C3 includes a plane view of a DRAM array and a section view along the line 7C3. Fig. 7C4 includes a plane

view of a CMOS flip-flop layout, a section view along the line 7C4 and the CMOS flip-flop circuit. In order that readers can sufficiently understand the new structure, Fig. 7C5 gives a different section view along the line 7C5 of the same structure shown in Fig. 7C4. Fig. 7C6 includes a plane view of a CMOS NAND layout, a section view along the line 7C6 and the CMOS NAND circuit. Fig. 7C7 gives a different section view along the line 7C7 of the same structure shown in Fig. 7C6. The size of PMOS is larger than that of NMOS in Fig. 7C6 and 7C7. $((W_P/L_P)/(W_N/L_N))$ of PMOS to NMOS is two. This ensures that PMOS has the same current drivability as NMOS. Fig. 7C8 shows a CMOS NAND layout with a minimum PMOS size.

(4) After the gate electrodes and word lines are formed, Si_3N_4 film 80 is deposited and etched selectively and anisotropically to form sidewall spacers 80 by familiar means. Formation the sidewall spacers 80 is an very important process step for achieving high density circuits and reducing the complexity of thefabrication process. This is a major improvement based on the structure and process shown in Fig. 6A-6K. Thereafter, SiO_2 11 is deposited by PECVD and planarized, followed by a selectively anisotropic plasma etching. The selective etching guarantees that only SiO_2 (the dielectrics 11 and 207) is etched and that silicon (the regions 5, 9, 51, 201 and 205) and the Si_3N_4 80 are not etched, or only slightly etched. The selective etching with the seventh mask forms five different deep contact holes 61 (Figs. 7D-7D10). The five different deep contact holes includes the top and sidewall contacts of the source or drain regions 5 and 51 of NMOS and PMOS, the top and sidewall contacts of the gate electrodes or word lines 9, and the top and sidewall contacts of the source or drain regions 201 and 205 of NMOS and PMOS. This selective etching saves four mask levels. Thereafter, polysilicon (single crystal silicon, polycide or refractory metal) 61 is deposited and etched back to remove excess polysilicon 61 on the upper surface of the dielectric 11. The polysilicon 61 is used not only as contact material, but also as interconnects. Thereafter, polysilicon (single crystal silicon, polycide or refractory metal) 62 is deposited, and Si_3N_4 63 is deposited on the polysilicon 62. The polysilicon 62 and Si_3N_4 63 are patterned simultaneously with the eighth mask to form the first level interconnects. Si_3N_4 film 64 is deposited and etched anisotropically to form sidewall spacers 64 by familiar means(Figs. 7D-7D1). Figs. 7D- 7D10 show the SRAM, full adder, DRAM, flip-flop, inverter chain and NAND layouts, at this stage in the fabrication process, respectively.

(5) SiO_2 66 is deposited by PECVD and planarized, followed by a selectively anisotropic plasma etching. The selective etching guarantees that only SiO_2 (the dielectrics 11, 66 and 207) is etched and silicon (the regions 5, 9, 51, 201 and 205) and Si_3N_4 (the dielectrics 63, 64 and 80) are not etched or only slightly etched. The selective etching with the ninth mask forms six different deep contact holes 67 (Figs. 7E-7E11). The six different deep contact holes includes the contacts of the polysilicon 61 (Figs. 7E4-7E11), the top and sidewall contacts of the source or drain regions

5 and 51 of NMOS and PMOS (Figs. 7E1 and 7E3-7E5), the top and sidewall contacts of the gate electrodes or word lines 9 (Figs. 7E-7E2), the top and sidewall contacts of the source or drain regions 201 and 205 of NMOS and PMOS (Fig. 7E3). This selective etching saves five mask levels. Thereafter, polysilicon (single crystal silicon, polycide or refractory metal) 67 is deposited and etched back to remove excess polysilicon 67 on the upper surface of the dielectric 66. The Si_3N_4 63 and 64 protect the polysilicon 62 and 61 during the selective etching of SiO_2, so that polysilicon 67, 62 and 61 will not short-circuit. Figs. 7E and 7E1 reveal that two cross-coupled inverters are formed in a very small area. The thickness of the sidewall spacers 64, for the key to achieving an ultra dense SRAM array, can only determine the spacing between the first level interconnects 62 and the second level contact material 67. Thereafter, polysilicon (single crystal silicon, polycide or refractory metal) 73 is deposited and patterned with the tenth mask to form the second level interconnects. Figs. 7E- 7E11 show the SRAM, full adder, DRAM, flip-flop and NAND layouts respectively at this stage in the fabrication process. Fig. 7E6, 7E8, 7E9 and 7E11 show various layouts of NAND.

(6) SiO_2 76 is deposited by PECVD and planarized, followed by a selectively anisotropic plasma etching. The selective etching guarantees that only SiO_2 (the dielectrics 76, 66 and 11) is etched and polysilicon, polycide or metal (the regions 73, 67 and 61) and Si_3N_4 (the dielectrics 64 and 63) are, at most, only slightly etched. The selective etching with the eleventh mask forms four different deep contact holes 74 (Fig. 7F). The four different deep contact holes includes the top and sidewall contacts of the polysilicon 61, 67 and 73. This selective etching saves three mask levels. Thereafter, polysilicon (single crystal silicon, polycide or refractory metal) 74 is deposited and etched back to remove excess polysilicon 74 on the upper surface of the dielectric 76, thereafter polysilicon (single crystal silicon, polycide or refractory metal) 75 is deposited. Thereafter, dielectric (SiO_2 or Si_3N_4) 216 is deposited on the polysilicon 75 and patterned with the twelfth mask, and thereafter, dielectric (SiO_2 or Si_3N_4) 217 is deposited and etched anisotropically to the sidewall spacers (Fig. 7F). The distance between two sidewall spacers 217 is much smaller than a minimum lithographic line width. Fig. 7F1 gives a planar view of this stage in the fabrication process.

(7) The polysilicons 75, 74, 73, 67, and 61 are selectively etched using the dielectrics (SiO_2 or Si_3N_4) 216 and 217 as a mask. The dielectrics 80, 76, 66 and 11 are not etched, due to the selective etching. After the etching, the dielectrics 216 and 217 are selectively removed. Dielectrics 224 for capacitors are formed. The oxide/nitride/oxide is preferred here as the capacitor dielectric because of its excellent reliability. The n-type or p-type doped amorphous silicon 221, for formation of the capacitor plate, is deposited and planarized to fill into the very narrow spacings between storage nodes. Amorphous silicon is recrystalized to regular polysilicon by the annealing

(Fig. 7G) which follows.

(8) The amorphous silicon (or polysilicon) 221 and polysilicon 75 are patterned at the same time with the thirteenth mask, saving a mask level. The polysilicon 221 is used as the cell plate in the area of DRAM array. The combination of the polysilicons 221 and 75 is used as the third level interconnects in the area of logic circuits. The polysilicons 75, 74, 73, 67 and 61 are used as multiple level interconnects in the area of logic circuits, while they are used as the storage node in the area of DRAM array. This is the most important improvement based on the structure and process shown in Fig. 6A-6K. A very thick polysilicon 218 shown in Fig. 6J does not need to be deposited and planarized. Therefore, it is not necessary for the thick polysilicon 218 to be planarized to a global thickness uniformity of 10% over the wafer. Thereafter, dielectric (SiO_2) 222 is deposited by PECVD. The first level global metal interconnect contact holes 223 and interconnects 260 are formed with the fourteenth and fifteenth masks (Fig. 7H). The second level global metal interconnect contact holes and interconnects are formed with the sixteenth and seventeenth masks. This step, however, is not diagrammed. The storage capacitors may be sufficiently large to satisfy the requirements of different level DRAMs through changing the heights of the polysilicons 61, 67, 73, 74 and 75. Fig. 7H1 gives a planar view of the smallest SRAM cell layout in the world with a minimum of 40 lithographic squares cell size. Figs. 7H2-7H3 give different section views along the lines 7H2 and 7H3 respectively of the same structure shown in Fig. 7H1. Figs. 7H4-7H10 include plane and section views of the full adder, flip-flop and NAND structures respectively.

Embodiment 3 (Figs. 6A-7H10) has the following major advantages over conventional device structures and fabrication processes.

1) Ultra dense DRAM arrays with a minimum of 4 lithographic squares cell size, the highest density full single crystal silicon 6-T SRAM arrays with a minimum of 40 lithographic squares cell size, and extremely high density logic circuits are integrated on the same chip. The new device with a channel width to length ratio (W/L) larger than 4 can be built in the smallest area within all the devices, therefore, this device is suitable for both high density and high speed integrated circuits.

2) Since the bit lines are below the transistors, the storage nodes may be built on the transistors. This eliminates trench-to-trench punch through the leakage current because the insulators completely surround the storage nodes.

3) Since the spacing between two neighboring storage nodes is much smaller than a minimum lithographic line width, the storage nodes occupy nearly all the area of a DRAM array. This

makes the size of trench capacitors achieve a maximum limit at a given trench height (or depth). Large capacitor and small leakage current lead to high soft-error resistance.

4) The storage nodes of DRAMs are made up of multiple level interconnects, reducing surface irregularity, and the complexity of the fabriction process.

5) Since selective etching, the doping effect of the etching, the sidewall spacers (Si_3N_4) 80, the protective layers (Si_3N_4) 63 and 64 of the polysilicon 62 are used and the polysilicons 75 and 221 are patterned simultaneously, 14 mask levels are saved, and can be used for vertical-transistor integrated circuits. This improvement reduces complexity of the fabrication process of the vertical devices, and solves the wiring problem that makes it difficult to form interconnects between vertical transistors. The new process shown in Fig. 7A-7H10 is also more simple than the advanced planar device processes. For example, high density planar transistor SRAM, quadruple or quintuple-level polysilicon, requires double-level metal and 23 mask levels. However, any metals from single to multi-level metals and 17 mask levels are used in the new process.

6) The major point to be clarified in explaining this embodiment is that access transistors of DRAM, driving, load and access transistors of SRAM, periphery CMOS transistors and CMOS logic transistors are vertical transistors and can be integrated on a single chip with the same gate and channel lengths. However, only specific vertical transistors can do this integration because a plurality of devices, especially the conventional devices, cannot satisfy all the requirements of different kinds of devices at the same time. For example, access transistors of DRAM need low leakage current. Devices which have suffered from short-channel effect cannot be access transistors. Access transistors need a relaxed channel length. On the other hand, periphery transistors and logic transistors need a short channel length to achieve high speed and high driving ability. No conventional vertical MOSFET can provide a solution. Second, no conventional vertical MOSFET structures, such as VMOS, UMOS and vertical IGFET, can form high performance buried-channel PMOS in CMOS circuits, because their doping profiles, vertical to the channel length, are uniform. The channel region has the same doping concentration as the body region in any conventional vertical MOSFET. leading to high threshold voltage in the channel region and low punch through resistance, unacceptable for device operation. Any conventional vertical sandwiched MOSFET suffers from short-channel effect due to large source/drain junction depth combined with down-scaling of device, since shallow and lightly doped source/drain extension regions do not exist in any conventional vertical MOSFET. In addition, conventional vertical MOSFET suffers from non-uniformity. Finally, it is very important that the wiring problem of vertical transistors could not be solved before the present invention, characterized by the new fabrication processes of interconnects. The above discussion includes major reasons why

vertical MOSFETs are not widely used in modem integrated circuits. New vertical transistors in the present invention solve all the drawbacks of conventional vertical transistors. They are superior to any planar transistor and any other vertical transistor in the world. They are the most promising candidates for future ultra-dense integrated circuits.

A new DRAM structure and process based on the structure and process in Fig.7A-7H10 is shown in Fig. 8A-8J, revealing a further increase in the storage capacitor size of DRAM.

(1) After polysilicon (polycide or refractory metal) 75 is deposited (Fig. 7F), SiO_2 film 251 is deposited on the polysilicon 75. Polysilicon (polycide or refractory) 252 is deposited on the SiO_2 film 251. Thereafter, the SiO_2 251 and polysilicon 252 are layered as such repeatedly (Fig. 8A). Dielectric (SiO_2) 250 is deposited and patterned, and dielectric (Si_3N_4) 253 is deposited and etched anisotropically to form sidewall spacers (Fig. 8B). Fig. 8B1 gives planar views of the structure shown in Fig. 8B. The SiO_2 251, polysilicon 252 and 75 are etched anisotropically using the dielectric 250 (SiO_2) and sidewall spacers (Si_3N_4) 253 as a mask. In order to protect the parts of the polysilicon 252 under the dielectric 250 (SiO_2) that should not be etched, the thickness of the dielectric 250 (SiO_2) is larger than the total thickness of multiple-level dielectric films 251 (SiO_2). However, this is not shown in the diagrams. Then amorphous silicon 254 is deposited and etched back by a selective etching to fill the narrow trenches (Fig.8C). The amorphous silicon 254 can be recrystalized to regular polysilicon by any heat cycle after deposition.

(2) The remaining dielectric 250 (SiO_2) is removed by selectively wet etching (Fig. 8D). For example, hydrofluoric acid (HF) attacks SiO_2 but leaves Si and Si_3N_4 unaffected at room temperature. After the dielectric 250 is removed, dielectric (Si_3N_4) 255 is deposited and etched anisotropically to form sidewall spacers (Fig. 8E). Fig. 8E1 gives planar views of the structure shown in Fig. 8E.

(3) The SiO_2 251 and polysilicon 252 are etched anisotropically using the sidewall spacers (Si_3N_4) 253 and 255 as a mask. The etching does not go through the polysilicon 75. The sidewall spacers (Si_3N_4) 253 and 255 may also be partly etched. The SiO_2 251 is removed by selectively wet etching (Fig. 8F). Thereafter the polysilicon 75, 74, 73, 67 and 61 are etched selectively and anisotropically. The dielectrics (Si_3N_4 and SiO_2) 80, 76, 66 and 11 are not etched (Fig. 8G). This process order is very important, so that the SiO_2 251 and polysilicon 252 may be etched first, and thereafter the SiO_2 251 removed and the polysilicon 75, 74, 73, 67 and 61 finally etched; this process order ensures that the SiO_2 76, 66 and 11 are not removed when the SiO_2 251 is removed by wet etching.

(4) After the polysilicon 75, 74, 73, 67 and 61 are etched, the remaining parts of dielectrics (Si_3N_4) 253 and 255 are selectively removed by slight plasma etching. The dielectrics (SiO_2) 76, 66 and 11 are not etched due to the selective etching; the dielectric (Si_3N_4) 80 is not completely removed for two reasons. One is that the etching rate is higher near the top of the high-aspect-ratio trench than near the bottom due to the reduced transport of reactants to the bottom of the trench as well as the reduced transport of the products away from the bottom of the trench. Second, the dielectrics (Si_3N_4) 253 and 255 can be completely removed by only slight plasma etching since most parts of dielectrics (Si_3N_4) 253 and 255 have been etched during the trench etching. Thereafter, dielectrics 224 for capacitors are formed. The oxide/nitride/oxide is preferred here as the capacitor dielectric because of its excellent reliability. Thereafter, the n-type or p-type doped amorphous silicon 221 is deposited and planarized to fill into the very narrow spacings between storage nodes, in order to form the capacitor plate. Amorphous silicon is recrystalized to regular polysilicon by the annealing (Fig. 8H) which follows.

(5) The amorphous silicon (or polysilicon) 221 and polysilicon 75, 252 and 254 are patterned at the same time with a mask. This saves a mask level. The polysilicon 221 is used as the cell plate in the area of DRAM array. The combination of the polysilicon 254, 252, 221 and 75 is used as the third level interconnects in the area of logic circuits. The polysilicon 254, 221, 75, 74, 73, 67 and 61 are used as multiple level interconnects in the area of logic circuits, while they are used as the storage node in the area of DRAM array. Thereafter, dielectric (SiO_2) 222 is deposited by PECVD (Fig. 8I). Finally, the global metal interconnects 260 and contact holes 223 are formed (Fig. 8J).

Since the multiple layers 252 are interconnected by the polysilicon 254 in a sublithographic contact hole and DRAM cells (or storage nodes) are separated by sublithographic features, the new cell shown in Fig. 8A-8J is named the SIC cell (Sublithographic Interconnects and isolation Cell). The SIC cell possesses a larger surface area of its storage electrode than does either the trench capacitor cell or stacked capacitor cell, and also a smaller cell leakage current and a higher soft-error resistance than the trench capacitor cell.

A new DRAM structure and process is proposed in Fig. 8K-8N, which reveals how we can increase storage capacitor size of the type of DRAM shown in Fig. 7A-7H10.

(1) After polysilicon (polycide or refractory metal) 75 is deposited (Fig. 7F), dielectric (SiO_2) 216 is deposited and patterned. Thereafter, dielectric (Si_3N_4) 217 is deposited and etched anisotropically to form sidewall spacers. Dielectrics 216 and 217 must be different materials. The polysilicon 75 are etched anisotropically using the dielectric 216 (SiO_2) and sidewall spacers (Si_3N_4) 217 as a mask (Fig. 8K).

(2) After the polysilicon 75 are etched, the dielectric (SiO_2) 216 in the areas of DRAM arrays is selectively and locally removed with the thirteen masks (Fig. 8L). The dielectric (Si_3N_4) 217 and polysilicon 75 are not etched while selectively etching the dielectric (SiO_2) 216. Fig. 8L1 gives planar views of the structure shown in Fig. 8L.

(3) The polysilicon 75, 74, 73, 67 and 61 are etched anisotropically and selectively using the remaining dielectric 216 (SiO_2) and sidewall spacers (Si_3N_4) 217 as a mask (Fig. 8M). Due to the two-step etching process, different deep trenches are formed. The deeper trenches are used to isolate the different storage nodes; the more shallow trenches are used to increase the area of the storage node. If the two-step etching process is not used, the trench etching may reach the lightly doped source/drain region 4 and the body regions 3 and 32 through the heavily n-doped source/drain region 5. After the trench etching, the dielectrics 216 and 217 are selectively removed, and thereafter, the dielectrics 224 for capacitors are formed. The oxide/nitride/oxide is preferred here as the capacitor dielectric because of its excellent reliability. Thereafter, the n-type or p-type doped amorphous silicon 221 is deposited and planarized to fill into the very narrow spacings between storage nodes, in order to form the capacitor plate. Amorphous silicon is recrystalized to regular polysilicon by the annealing (Fig. 8M) which follows.

(4) The amorphous silicon (or polysilicon) 221 and polysilicon 75 are patterned at the same time with the fourteenth mask. This saves a mask level. The polysilicon 221 is used as the cell plate in the area of DRAM array. The combination of the polysilicon 221 and 75 is used as the third level interconnects in the area of logic circuits. The polysilicon 75, 74, 73, 67 and 61 are used as multiple level interconnects in the area of logic circuits, while they are used as the storage node in the area of DRAM array. Thereafter, dielectric (SiO_2) 222 is deposited by PECVD. The global metal interconnect contact holes 223 and interconnects 260 are formed with the fifteenth and sixteenth masks (Fig. 8N).

Figs. 9A-9C give a modified structure and process based on the structure and process in Fig. 7A-7H10. It is illustrated in Fig. 9A-9C that trench capacitor DRAM array are integrated with logic circuits. The process consists of the following steps:

(1) A heavily n-type doped layer 273 and a very lightly n-type doped layer 270 are first formed respectively by the in-situ doping epitaxy method on a heavily p-doped silicon substrate 1 (Fig. 9A). Thereafter, the regions 201, 205, 271, 272 and 274 are formed by ion-implantation (Fig. 9B).

(2) Undoped silicon layer 152 is epitaxied on the regions 201, 205 and 272., and afterwards, Si_3N_4 27 is deposited on the layer 152. The Si_3N_4 and undoped silicon layer 152 are patterned with the second mask. After the patterning, thin SiO_2 layer 21 is grown on the silicon surface by thermal oxidation. The SiO_2 sidewall spacers 21 are formed by selectively anisotropic etching (Fig. 6C). Three different deep trenches are engraved into the regions 1, 201, 205, 270, 271, 272, 273 and 274 by plasma etching. The formation of the three different deep trenches with only one mask and one etching is due to the the doping effect of the etching. If the trenches are formed by Cl atom plasma etching, using one among such gases as Cl_2, Cl_2+Ar, CCl_4+Ar, CF_3Cl, $SiCl_4+O_2$, CF_3Br+Cl_2 or $C_2F_6+Cl_2$ as an etchant gas, the etching rate of the heavily n-doped regions 201, 272 and 273 is 15-25 times larger than that of the very lightly doped regions 270. Since p-type dopants suppress silicon etch rates, the etching rate of the regions 1, 205, 271 and 274 is lower than that of the very lightly doped regions 270. This process saves two mask levels. After the trench etching, all the exposed silicon surfaces are cleaned, and dielectrics for capacitors are formed on the trench surfaces. Thereafter, polysilicon or amorphous silicon 6 is deposited and planarized over the wafer. The silicon 6 is selectively etched back to a proper depth to fill the trench to form the cell plate of the storage capacitor. Thereafter, thick SiO_2 17 is deposited by PECVD and then planarized and etched back to a proper depth by selectively anisotropic etching to fill the trenches (Fig. 9C).

Since the following process steps are very similar to those shown in Fig. 7A-7H10, they are mentioned and diagrammed again.

Embodiment 4:

Figs. 10A-10G1 are plane and section views illustrating the steps in a process for producing 2-F DRAM cells. The process consists of the following steps:

(1) A heavily n-type doped layer 2 is first formed by the in-situ doping epitaxy method on a heavily p-doped silicon substrate 1. Undoped silicon 152 is epitaxied on the heavily n-type doped layer 2. Dielectric (Si_3N_4 or SiO_2) 27 is deposited on the undoped silicon 152. The dielectric 27, undoped silicon 152, heavily n-type doped layer 2 and part of substrate 1 are patterned with a checkered layout of mask 150 (Fig. 10A). The spacing between the corners of silicon pillars is narrower than the design rule. The narrow spacing can be well controlled by exposure time in a lithography process (Fig. 10B).

(2) After the trench etching, all the exposed silicon surfaces are cleaned; dielectrics for capacitors are formed on the trench surfaces. Thereafter, heavily n-doped polysilicon or amorphous silicon 6 is deposited and planarized over the wafer. The silicon 6 is selectively etched

back to a proper depth to fill the trench to form the cell plate of the storage capacitor. Thereafter, a relative thick SiO_2 8 is formed on the surface of the heavily n-doped polysilicon 6 and a relative thin SiO_2 8 is formed on the surface of the undoped silicon 152 at the same time by using the method of concentration-enhanced oxidation. The relative thin SiO_2 8 is used as a gate insulator. Polysilicon or amorphous silicon film 9 is deposited over the wafer and patterned with the second mask 170 (Fig. 10C). Thereafter, dielectric (SiO_2) 10 is deposited and etched back (Fig. 10D). The polysilicon 9 is etched anisotropically to form gate electrodes and word lines and the dielectric 10 may also be partially etched. This needs to choose the selective etching rate ratio between the polysilicon and dielectric. The dielectric 10 must protect the bottom portion of the polysilicon 9 not to be etched (Fig. 10E). The shape of the combination of gate electrodes and word lines is the most important in the embodiment.

(3) After the gate electrodes and word lines are formed, lightly n-doped source/drain regions 4, the p-doped channel or body region 3 and heavily n-doped source/drain region 5 are formed by ion implantation. The source/drain and channel regions may, of course, be formed before the gate electrodes and word lines are formed. The shallow source/drain extension regions, low threshold channel region and high punch-through resistance body region are not diagrammed. Thereafter, the dielectric (SiO_2) 11 is deposited and etched back to a proper depth, and afterwards, a self-aligned silicide ($TiSi_2$) 162 is formed on the heavily n-doped source/drain region 5. Thereafter, the metal (polysilicon or polycide) 12 is deposited over the wafer. Silicide ($TiSi_2$) 163 is formed on the metal 12 (This step is not necessary). Thereafter, dielectric 154 is deposited and patterned. The line width of the dielectric 154 is a little smaller than the minimum feature size on the mask. This is well controlled by the exposure time during the lithography process. Thereafter, dielectric 155 is deposited and etched anisotropically to form sidewall spacers (Fig. 10F). The dielectrics 154 and 155 must be different materials. Fig. 10F1 gives another section view along the different line 10F1 of the same structure shown in Fig. 10F.

(4) After the sidewall spacers are formed, the dielectric 154 is selectively removed by wet etching. The silicide 163 and metal 12 is patterned by using the sidewall spacers 155 as a mask. It is preferred that selective etching is used when the metal 12 is patterned because the silicide 162 and silicon 5 are not etched or are only slightly etched. Fig. 10G1 gives another section view along the different line 10G1 of the same structure shown in Fig. 10G.

Figs. 10H-10K give another method to form the bit lines of the 2-F cells. The process consists of the following steps:

(1) After a self-aligned silicide ($TiSi_2$) 162 is formed, metal (alloy, polysilicon or polycide) 12,

silicide 163 and dielectric 170 are deposited over the wafer and patterned to form the first bit lines. It is preferred that selective etching is used when the metal 12 is patterned (Fig. 10H).

(2) Dielectric 171 is deposited and etched anisotropically to form sidewall spacers (Fig. 10I). It is preferred that the dielectrics 170 and 171 are different materials because the sidewall spacers may be lower than the dielectric 170 when selective etching is used (Fig. 10J).

(3) Finally, metal (alloy, polysilicon or polycide) 172 is deposited and etched back to remove excess metal 172 on the upper surface of the dielectric 170 to form the second bit lines (Fig. 10K).

The novel layout of gate electrodes and word lines 9 is a key to achieve the 2-F cell. The gate electrode 9 surrounds a half of the silicon pillar island and the gate electrodes are self-aligned connected together to form the word lines (Fig. 10E). It is better to understand the novel layout that readers carefully see the structures shown in the diagrams. The 2-F cell is the second smallest DRAM cell in the world. It is used for 1 Gbit DRAM production with 0.3 μm design rule, thus it can pave the way to the giga-bit DRAM era. However, any planar access transistor cell will not be smaller than 6 minimum lithographic squares (or 6 feature sizes) because the source, channel (or gate) and drain regions must occupy at least 3 feature sizes when misregistration is considered. For the vertical transistor, the source, channel (or body) and drain regions are overlapped and they occupy only one feature size. If the wiring problems (including the layouts of word lines, bit lines and interconnects) are solved, vertical transistors are absolutely superior to planar transistors. Device development towards three dimensions is a positive trend.

Embodiment 5:

Figs. 11A-11I are plane and section views illustrating the steps in a process for producing 1-F DRAM cells. The process consists of the following steps:

(1) A heavily n-type doped layer 2 is first formed by the in-situ doping epitaxy method on a heavily p-doped silicon substrate 1. Undoped silicon 152 is epitaxied on the heavily n-type doped layer 2. Dielectric (Si_3N_4) 27 is deposited on the undoped silicon 152. The dielectric 27 and undoped silicon 152 are patterned with a checkered layout of mask 150 (Fig. 11A). The spacing between the corners of silicon pillars is narrower than the design rule. The narrow spacing can be well controlled by exposure time in the lithography process. After the patterning, SiO_2 layer 21 is grown on the silicon surface by thermal oxidation. The perimeter of the silicon pillar islands is reduced. Then the SiO_2 sidewall spacers 21 are formed by selectively anisotropic etching using CF_4+H_2, CCl_2F_2, C_4F_8, HF or CHF_3 as an etchant gas in a familiar way. The trench etching mask Si_3N_4 27 is not etched, or only slightly etched. The SiO_2 sidewall spacers 21 not only

protect the channel region of devices from the second relative deep trench etching, but also make it so that the area of the horizontal cross section of the upper portion of the silicon pillar island be smaller than a minimum lithographic square. The second relative deep trenches are engraved into the heavily p-doped substrate 1 (Fig. 11B). After the trench etching, all the exposed silicon surfaces are cleaned. Thereafter, the dielectrics 7 for storage capacitors are formed. Thereafter, the heavily n-type doped polysilicon or amorphous silicon 6 is filled in the trenches to form the capacitor plates. The Si_3N_4 27 and SiO_2 sidewall spacers 21 are selectively removed by wet etching, after which all the exposed silicon surfaces are cleaned. The gate insulator 8 is formed and the heavily n-doped polysilicon 9 is deposited and etched anisotropically to form polysilicon sidewall gate electrodes (Fig. 11C). The polysilicon sidewall gate electrodes are lower than the silicon region 152. It is due to the use of the doping effect of etching. If Cl_2, Cl_2+Ar, CCl_4+Ar, CF_3Cl, $SiCl_4+O_2$, CF_3Br+Cl_2 or $C_2F_6+Cl_2$ is used as an etchant gas, the etching rate of the heavily n-doped polysilicon 9 is 15-25 times higher than that of the undoped silicon region 152, so using the doping effect of etching is a key to forming the buried gate transistor in this embodiment.

(2) The sidewall gate electrodes have been formed, but how can the sidewall gate electrodes be smartly connected together to form word lines? This is a very important problem for the formation of the 1-F cell.

A relatively thin dielectric (Si_3N_4) film 156 is formed on all the exposed silicon surface, Thereafter a relative thick dielectric (SiO_2) is deposited and etched selectively and anisotropically to form sidewall spacers. It is preferred that the dielectrics 156 and 157 are different materials because this ensures that selective etching may be used; thereafter, the heavily n-doped polysilicon 6 is etched by using the undoped silicon 152 and dielectrics 156 and 157 as a mask. Cl_2, Cl_2+Ar, CCl_4+Ar, CF_3Cl, $SiCl_4+O_2$, CF_3Br+Cl_2 or $C_2F_6+Cl_2$ must be used as an etchant gas to etch the heavily n-doped polysilicon 6. This ensures that the undoped silicon 152 is not etched, or only slightly etched (Fig. 11D).

(3) After the heavily n-doped polysilicon 6 is etched, all the exposed silicon surfaces are cleaned. Thereafter, the dielectrics 199 for storage capacitors are formed, and the heavily n-type doped polysilicon or amorphous silicon 14 is deposited and etched back to a proper depth to fill the trenches. A relative thick SiO_2 167 is formed on the heavily n-type doped polysilicon 14 and a relative thin SiO_2 167 is formed on the undoped silicon region 152 by using the method of concentration-enhanced oxidation. The dielectric 167 may, of course, be Si_3N_4. Thereafter, heavily n-type doped polysilicon or amorphous silicon 159 is deposited and planarized. Thereafter, dielectric (SiO_2) 154 is deposited and patterned. Dielectric (Si_3N_4) 155 is deposited and etched anisotropically to form sidewall spacers (Fig. 11E).

(4) The dielectrics 154 and 156 must be different materials to ensure that the dielectric 154 may be selectively removed by wet etching. After the dielectric 154 is removed, dielectric (Si_3N_4) 158 is deposited and etched anisotropically to form sidewall spacers. The heavily n-type doped polysilicon 159 is etched by using the dielectrics 155 and 158 as a mask and using Cl_2, Cl_2+Ar, CCl_4+Ar, CF_3Cl, $SiCl_4+O_2$, CF_3Br+Cl_2 or $C_2F_6+Cl_2$ as an etchant gas. Using sidewall spacers 155 and 158 as a mask is an important method of sublithographic patterning. Even if the thin dielectric (SiO_2 or Si_3N_4) 167 on the undoped silicon 152 is removed by the above etching, the undoped silicon 152 is at most, only slightly etched since the doping effect of plasma etching is used. The above etching does not affect the dielectric (Si_3N_4) 155, 156 and 158 and dielectric (SiO_2) 157 because Cl atom plasma gives a high selective etching ratio for Si : Si_3N_4 or SiO_2. Therefore, the dielectric (SiO_2) 157 protects the sidewall polysilicon gate electrode, and thus the sidewall polysilicon gate electrode protects the gate oxide. Thereafter, the dielectric (SiO_2) 157 is etched selectively and anisotropically. The selective etching ensures that the undoped silicon 152, heavily n-doped polysilicon 9 and 159 and the dielectrics (Si_3N_4) 155, 156 and 158 are at most, only slightly etched.The purpose of the two-step etching of polysilicon 159 and dielectric 157 is to ensure that the heavily n-doped polysilicon gate electrodes 9 and undoped silicon region 152 are only slightly etched. Figs. 11F and 11F1 show a plane view and two section views along the different lines 11F and 11F1 at the stage in the fabrication process. The purpose of the deposition of the heavily n-type doped polysilicon 159 is to form a flat surface to form the sidewall spacers 155 and 158. In addition, the heavily n-type doped polysilicon 159 can be selectively etched on the undoped silicon 152, dielectrics (Si_3N_4) 155, 156 and 158 and dielectric (SiO_2) 157. It is better for understanding the fabrication step that readers carefully observe Figs. 11E, 11F and 11F1.

(5) The dielectric (Si_3N_4) 156 is selectively removed. Even if the dielectrics 156 and 167 are the same materials, it does not matter because the polysilicon 159 protects the dielectric 167. The heavily n-type doped polysilicon 159 is deposited again and selectively etched back to a proper depth by using the doping effect of plasma etching. Figs. 11G and 11G1 show a plane view and two section views along the different lines 11G and 11G1 at this stage in the fabrication process. At one point in the fabrication process, the sidewall gate electrodes 9 can be connected together by the heavily n-doped polysilicon 159 to form the word lines.

(6) Dielectric (SiO_2 or Si_3N_4) 160 is deposited and anisotropically etched to form sidewall spacers. Thereafter, the heavily n-doped polysilicon 159 is etched by using the undoped silicon region 152 and sidewall spacers 160 as a mask and using the doping effect of plasma etching. Thereafter, the dielectric (SiO_2) 167 is selectively etched. The SiO_2 198 is formed on the surface of the polysilicon 159 and 14 by thermal oxidation. The SiO_2 198 on the surface of the polysilicon 14

is etched by anisotropic etching. The SiO_2 198 on the surface of the polysilicon 159 remains since the etching is anisotropic (Fig. 11H). If the dielectric 167 is Si_3N_4, the SiO_2 198 is first formed on the surface of the polysilicon 159, then the dielectric 167 is selectively etched by wet etching. The selective wet etching does not attack the SiO_2 198. Fig. 11H1 gives another section view along the line 11H1 of the same structure shown in Fig. 11H.

(7) Amorphous 161 silicon is deposited over the wafer and planarized to fill narrow spacings between the SiO_2 198, followed by multiple ion implants. The multiple ion implants form lightly n-doped source/drain regions 4, source-to-drain nonuniformly p-type doped channel (or body) regions 31, 32 and 33, and heavily n-doped source/drain regions 5. An annealing activates the implanted impurities and recrystallizes amorphous silicon to regular polysilicon. The multiple ion implants form the source/drain and channel regions of single crystal MOSFETs and simultaneously form source/drain and channel regions of polysilicon MOSFETs located between the SiO_2 198. The narrowness of the channel (or body) region of the polysilicon MOSFETs is the reason that this device is called a nail transistor (NT). Due to very narrow channel region (smaller than 0.01 μm^2) and relative long channel length, the leakage current of the NT is dramatically reduced and the gate voltage control ability is improved. Thereafter, silicide 162 is formed on the polysilicon 161. The thermal cycle of forming silicide may serve the purpose of activating impurities and recrystallizing amorphous silicon. Metal 12 is deposited, followed by depositing another kind of metal (or polycide, nitride, polysilicon, alloy) 163. Metals 163 and 12 and silicide 162 are patterned by the method of sublithographic patterning (Fig. 11I). Fig. 11I1 gives another section view along the line 11I1 of the same structure shown in Fig. 11I.

Fig. 12 illustrates that it is not important that the polysilicon 6 is over etched.

Fig. 13 shows a modified structure based on the structure in Fig. 12. The difference is that the dielectric 199 on the substrate 1 is removed by anisotropic etching and the dielectric 199 on the surface of the polysilicon 6 remains.

Due to the dramatic reduction of device size, all the single crystal MOSFETs may be replaced by the polysilicon nail transistors (NTs) because the nail transistors have very low leakage currents. The NT can be used to form multiple-level device structures (Fig. 14). Polycrystalline diamond film 165 are formed between two levels devices by plasma enhanced chemical vapor deposition (PECVD). Polycrystalline diamond film has high thermal conductivity and electrical resistance. Therefore, polycrystalline diamond film is used as insulating material between devices to overcome the power limit of future ultra-large integrated circuits. The very thin dielectric 164 is used as a buffer layer to reduce diffusion between different materials and improve isolation

between different-level devices. (This step is not necessary). In general, the development of integrated circuits will be unlimited.

Figs. 15A-15B1 illustrate that a 2-F DRAM array can be fabricated by using the structure and process of 1-F cell shown in Figs. 11A-11I1. The difference is that the polysilicon 6 is not etched and nail transistors are not formed. Comparing Fig. 15B and 15B1 with Figs. 11G and 11G1, the 2-F cell structure and process may be easily understood. The major advantage of 2-F cell is the relatively simple fabrication process. The formation of bit lines of the 2-F cell do not need the method of sublithographic patterning. Fig. 15C gives a structure of floating-body free 2-F cell.

Finally, it should be appreciated that various modifications may be made without departing from the spirit and scope of the invention. In particular, the various temperatures, dimensions, doping concentrations, ion-implantation doses and energies, etchants, device types, material types, and geometric shapes of devices mentioned are merely illustrative. Silicon, SiO_2 or Si_3N_4 may be replaced by other semiconducting and insulating materials. Doped polysilicon and single crystal silicon, polycide or metal may be replaced by other material which has a small resistivity, for example, refractory metal, low melting point metal (Al or Al alloy), silicides, nitrides, carbides, borides, doped poly-crystal materials, doped single-crystal materials, and superconducting materials.

4 Brief Description of Drawings

Fig. 1A is plane and section views illustrating a first embodiment of the present invention.

Fig. 1B is plane and section views illustrating a first embodiment of the present invention.

Fig. 1C is plane and section views illustrating a first embodiment of the present invention.

Fig. 1D is plane and section views illustrating a first embodiment of the present invention.

Fig. 1E is plane and section views illustrating a first embodiment of the present invention.

Fig. 1E1 is section views illustrating a first embodiment of the present invention.

Fig. 1F is plane and section views illustrating a first embodiment of the present invention.

Fig. 1G is plane and section views illustrating a first embodiment of the present invention.

Fig. 1G1 is plane and section views illustrating a first embodiment of the present invention.

Fig. 1G2 is plane and section views illustrating a first embodiment of the present invention.

Fig. 1G3 is plane and section views illustrating a first embodiment of the present invention.

Fig. 1G4 is plane and section views illustrating a first embodiment of the present invention.

Fig. 1H is plane and section views illustrating a first embodiment of the present invention.

Fig. 1H1 is plane and section views illustrating a first embodiment of the present invention.

Fig. 1H2 is plane and section views illustrating a first embodiment of the present invention.

Fig. 1H3 is plane and section views illustrating a first embodiment of the present invention.

Fig. 1H4 is plane and section views illustrating a first embodiment of the present invention.

Fig. 1I is plane and section views illustrating a first embodiment of the present invention.

Fig. 1I1 is plane and section views illustrating

a first embodiment of the present invention.

Fig. 1I2 is plane and section views illustrating a first embodiment of the present invention.

Fig. 1I3 is plane and section views illustrating a first embodiment of the present invention.

Fig. 1I4 is plane and section views illustrating a first embodiment of the present invention.

Fig. 1I5 is plane and section views illustrating a first embodiment of the present invention.

Fig. 1I6 is plane and section views illustrating a first embodiment of the present invention.

Fig. 1I7 is plane and section views illustrating a first embodiment of the present invention.

Fig. 1I8 is plane and section views illustrating a first embodiment of the present invention.

Fig. 1I9 is plane and section views illustrating a first embodiment of the present invention.

Fig. 1I10 is plane and section views illustratin g a first embodiment of the present invention.

Fig. 1I11 is plane and section views illustratin g a first embodiment of the present invention.

Fig. 1JA is plane and section views illustrating a first embodiment of the present invention.

Fig. 1JB is plane and section views illustrating a first embodiment of the present invention.

Fig. 1JC is plane and section views illustrating a first embodiment of the present invention.

Fig. 1JD is plane and section views illustrating a first embodiment of the present invention.

Fig. 1JE is plane and section views illustrating a first embodiment of the present invention.

Fig. 1K is plane and section views illustrating a first embodiment of the present invention.

Fig. 2A is plane and section views illustrating a second embodiment of the present invention.

Fig. 2B is plane and section views illustrating a second embodiment of the present invention.

Fig. 2C is plane and section views illustrating

a second embodiment of the present invention.

Fig. 2CA is plane and section views illustrating a second embodiment of the present invention.

Fig. 2CB is plane and section views illustrating a second embodiment of the present invention.

Fig. 2CC is plane and section views illustrating a second embodiment of the present invention.

Fig. 2D is plane and section views illustrating a second embodiment of the present invention.

Fig. 3 is section views illustrating a second embodiment of the present invention.

Fig. 4A is section views illustrating a second embodiment of the present invention.

Fig. 4B is section view illustrating a second embodiment of the present invention.

Fig. 5A is plane and section views illustrating a second embodiment of the present invention.

Fig. 5B is plane and section views illustrating a second embodiment of the present invention.

Fig. 5C is plane and section views illustrating a second embodiment of the present invention.

Fig. 5D is plane and section views illustrating a second embodiment of the present invention.

Fig. 5E is plane and section views illustrating a second embodiment of the present invention.

Fig. 5E1 is plane and section views illustrating a second embodiment of the present invention.

Fig. 5E2 is plane and section views illustrating a second embodiment of the present invention.

Fig. 5E3 is section view illustrating a second embodiment of the present invention.

Fig. 5E4 is section view illustrating a second embodiment of the present invention.

Fig. 5E5 is section view illustrating a second embodiment of the present invention.

Fig. 5E6 is section view illustrating a second embodiment of the present invention.

Fig. 5E7 is section view illustrating a second e

mbodiment of the present invention.

Fig. 5E8 is section view illustrating a second embodiment of the present invention.

Fig. 5E9 is section view illustrating a second embodiment of the present invention.

Fig. 6A is section view illustrating a third embodiment of the present invention.

Fig. 6B is section view illustrating a third embodiment of the present invention.

Fig. 6C is plane and section views illustrating a third embodiment of the present invention.

Fig. 6D is plane and section views illustrating a third embodiment of the present invention.

Fig. 6E is plane and section views illustrating a third embodiment of the present invention.

Fig. 6E1 is plane view and circuit diagram illustrating a third embodiment of the present invention.

Fig. 6E2 is plane and section views illustrating a third embodiment of the present invention.

Fig. 6E3 is plane and section views illustrating a third embodiment of the present invention.

Fig. 6F is plane and section views illustrating a third embodiment of the present invention.

Fig. 6F1 is plane and section views illustrating a third embodiment of the present invention.

Fig. 6G is plane and section views illustrating a third embodiment of the present invention.

Fig. 6G1 is plane and section views illustrating a third embodiment of the present invention.

Fig. 6G2 is plane and section views illustrating a third embodiment of the present invention.

Fig. 6H is plane and section views illustrating a third embodiment of the present invention.

Fig. 6H1 is plane and section views illustrating a third embodiment of the present invention.

Fig. 6I is section view illustrating a third embodiment of the present invention.

Fig. 6J is section view illustrating a third embodiment of the present invention.

Fig. 6J1 is plane view illustrating a third embodiment of the present invention.

Fig. 6K is section view illustrating a third embodiment of the present invention.

Fig. 7A is plane view illustrating a third embodiment of the present invention.

Fig. 7B is section view illustrating a third embodiment of the present invention.

Fig. 7C is plane and section views illustrating a third embodiment of the present invention.

Fig. 7C1 is plane view and circuit diagram illustrating a third embodiment of the present invention.

Fig. 7C2 is plane and section views illustrating a third embodiment of the present invention.

Fig. 7C3 is plane and section views illustrating a third embodiment of the present invention.

Fig. 7C4 is plane and section views, and circuit diagram illustrating a third embodiment of the present invention.

Fig. 7C5 is plane and section views illustrating a third embodiment of the present invention.

Fig. 7C6 is plane and section views, and circuit diagram illustrating a third embodiment of the present invention.

Fig. 7C7 is plane and section views illustrating a third embodiment of the present invention.

Fig. 7C8 is plane and section views, and circuit diagram illustrating a third embodiment of the present invention.

Fig. 7D is plane and section views illustrating a third embodiment of the present invention.

Fig. 7D1 is plane and section views illustrating a third embodiment of the present invention.

Fig. 7D2 is plane and section views illustrating a third embodiment of the present invention.

Fig. 7D3 is plane and section views illustrating a third embodiment of the present invention.
Fig. 7D4 is plane and section views illustrating a third embodiment of the present invention.
Fig. 7D5 is plane and section views illustrating a third embodiment of the present invention.
Fig. 7D6 is plane and section views illustrating a third embodiment of the present invention.
Fig. 7D7 is section view and circuit diagram illustrating a third embodiment of the present invention.
Fig. 7D8 is plane and section views illustrating a third embodiment of the present invention.
Fig. 7D9 is plane and section views illustrating a third embodiment of the present invention.
Fig. 7D10 is plane and section views illustrating a third embodiment of the present invention.
Fig. 7E is plane and section views illustrating a third embodiment of the present invention.
Fig. 7E1 is plane and section views illustrating a third embodiment of the present invention.
Fig. 7E2 is plane and section views illustrating a third embodiment of the present invention.
Fig. 7E3 is plane and section views illustrating a third embodiment of the present invention.
Fig. 7E4 is plane and section views illustrating a third embodiment of the present invention.
Fig. 7E5 is plane and section views illustrating a third embodiment of the present invention.
Fig. 7E6 is plane and section views illustrating a third embodiment of the present invention.
Fig. 7E7 is plane and section views illustrating a third embodiment of the present invention.
Fig. 7E8 is plane and section views illustrating a third embodiment of the present invention.
Fig. 7E9 is plane and section views illustrating a third embodiment of the present invention.
Fig. 7E10 is plane and section views illustratin

g a third embodiment of the present invention.

Fig. 7E11 is plane and section views illustrating a third embodiment of the present invention.

Fig. 7F is section view illustrating a third embodiment of the present invention.

Fig. 7F1 is section view illustrating a third embodiment of the present invention.

Fig. 7G is section view illustrating a third embodiment of the present invention.

Fig. 7H is section view illustrating a third embodiment of the present invention.

Fig. 7H1 is plane and section views illustrating a third embodiment of the present invention.

Fig. 7H2 is section view illustrating a third embodiment of the present invention.

Fig. 7H3 is section view illustrating a third embodiment of the present invention.

Fig. 7H4 is section view illustrating a third embodiment of the present invention.

Fig. 7H5 is section view illustrating a third embodiment of the present invention.

Fig. 7H6 is plane and section views illustrating a third embodiment of the present invention.

Fig. 7H7 is plane and section views illustrating a third embodiment of the present invention.

Fig. 7H8 is plane and section views illustrating a third embodiment of the present invention.

Fig. 7H9 is plane and section views illustrating a third embodiment of the present invention.

Fig. 7H10 is plane and section views illustrating a third embodiment of the present invention.

Fig. 8A is section view illustrating a third embodiment of the present invention.

Fig. 8B is section view illustrating a third embodiment of the present invention.

Fig. 8B1 is plane view illustrating a third embodiment of the present invention.

Fig. 8C is section view illustrating a third emb

odiment of the present invention.

Fig. 8D is section view illustrating a third embodiment of the present invention.

Fig. 8E is section view illustrating a third embodiment of the present invention.

Fig. 8E1 is plane view illustrating a third embodiment of the present invention.

Fig. 8F is section view illustrating a third embodiment of the present invention.

Fig. 8G is section view illustrating a third embodiment of the present invention.

Fig. 8H is section view illustrating a third embodiment of the present invention.

Fig. 8I is section view illustrating a third embodiment of the present invention.

Fig. 8J is section view illustrating a third embodiment of the present invention.

Fig. 8K is section view illustrating a third embodiment of the present invention.

Fig. 8L is section view illustrating a third embodiment of the present invention.

Fig. 8L1 is plane view illustrating a third embodiment of the present invention.

Fig. 8M is section view illustrating a third embodiment of the present invention.

Fig. 8N is section view illustrating a third embodiment of the present invention.

Fig. 9A is plane view illustrating a third embodiment of the present invention.

Fig. 9B is plane view illustrating a third embodiment of the present invention.

Fig. 9C is section view illustrating a third embodiment of the present invention.

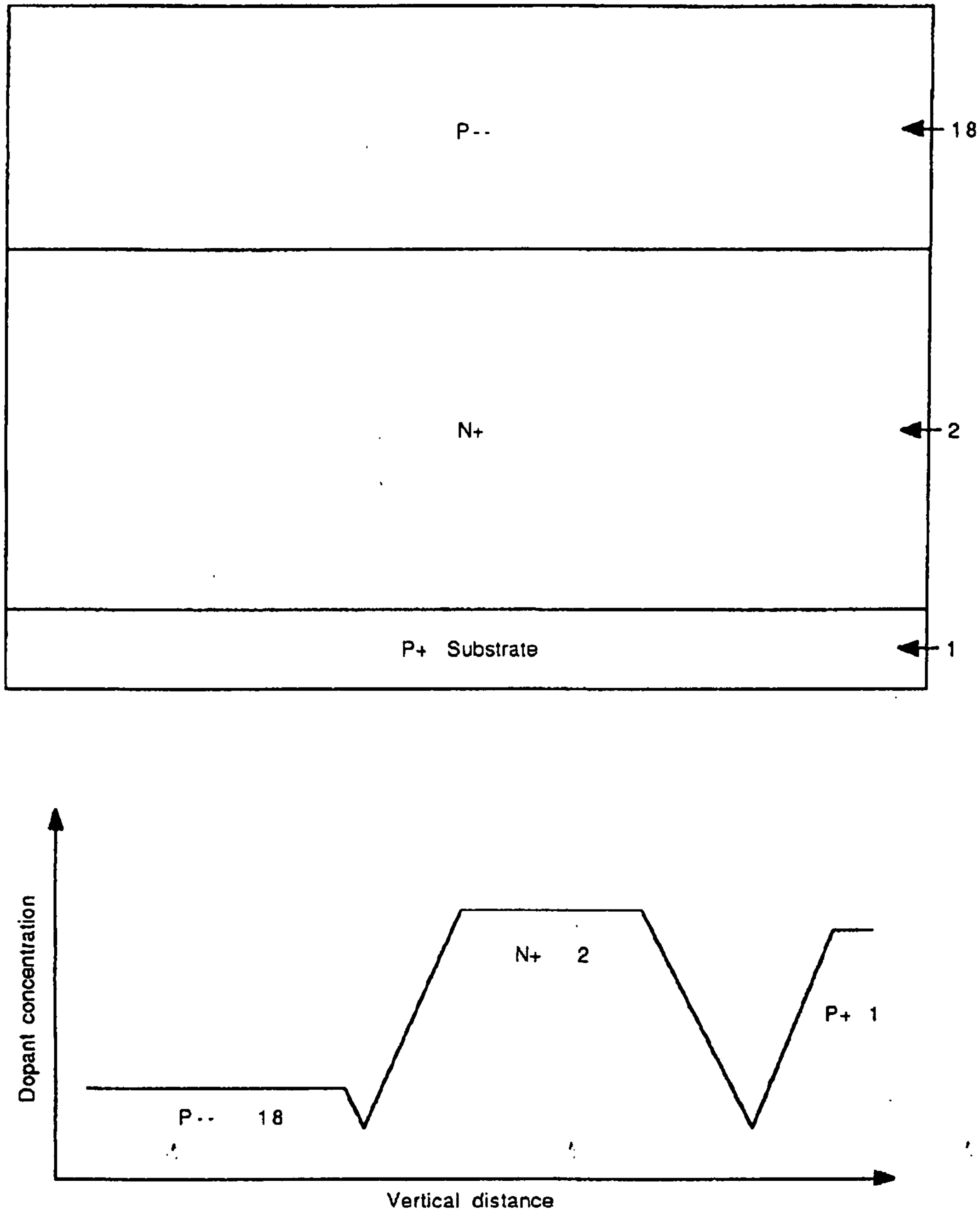
Fig. 10A is plane and section views illustrating a fourth embodiment of the present invention.

Fig. 10B is plane and section views illustrating a fourth embodiment of the present invention.

Fig. 10C is plane and section views illustrating

a fourth embodiment of the present invention.
Fig. 10D is plane and section views illustrating a fourth embodiment of the present invention.
Fig. 10E is plane and section views illustrating a fourth embodiment of the present invention.
Fig. 10F is plane and section views illustrating a fourth embodiment of the present invention.
Fig. 10F1 is plane and section views illustrating a fourth embodiment of the present invention.
Fig. 10G is plane and section views illustrating a fourth embodiment of the present invention.
Fig. 10G1 is plane and section views illustrating a fourth embodiment of the present invention.
Fig. 10H is plane and section views illustrating a fourth embodiment of the present invention.
Fig. 10I is plane and section views illustrating a fourth embodiment of the present invention.
Fig. 10J is plane and section views illustrating a fourth embodiment of the present invention.
Fig. 10K is plane and section views illustrating a fourth embodiment of the present invention.
Fig. 11A is plane and section views illustrating a fifth embodiment of the present invention.
Fig. 11B is plane and section views illustrating a fifth embodiment of the present invention.
Fig. 11C is plane and section views illustrating a fifth embodiment of the present invention.
Fig. 11D is plane and section views illustrating a fifth embodiment of the present invention.
Fig. 11E is plane and section views illustrating a fifth embodiment of the present invention.
Fig. 11F is plane and section views illustrating a fifth embodiment of the present invention.
Fig. 11F1 is plane and section views illustrating a fifth embodiment of the present invention.
Fig. 11G is plane and section views illustrating a fifth embodiment of the present invention.
Fig. 11G1 is plane and section views illustratin

g a fifth embodiment of the present invention.
Fig. 11H is plane and section views illustrating a fifth embodiment of the present invention.
Fig. 11H1 is plane and section views illustrating a fifth embodiment of the present invention.
Fig. 11I is plane and section views illustrating a fifth embodiment of the present invention.
Fig. 11I1 is plane and section views illustrating a fifth embodiment of the present invention.
Fig. 12 is plane and section views illustrating a fifth embodiment of the present invention.
Fig. 13 is plane and section views illustrating a fifth embodiment of the present invention.
Fig. 14 is plane and section views illustrating a fifth embodiment of the present invention.
Fig. 15A is plane and section views illustrating a fifth embodiment of the present invention.
Fig. 15B is plane and section views illustrating a fifth embodiment of the present invention.
Fig. 15B1 is plane and section views illustrating a fifth embodiment of the present invention.
Fig. 15C is plane and section views illustrating a fifth embodiment of the present invention.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P+ Substrate
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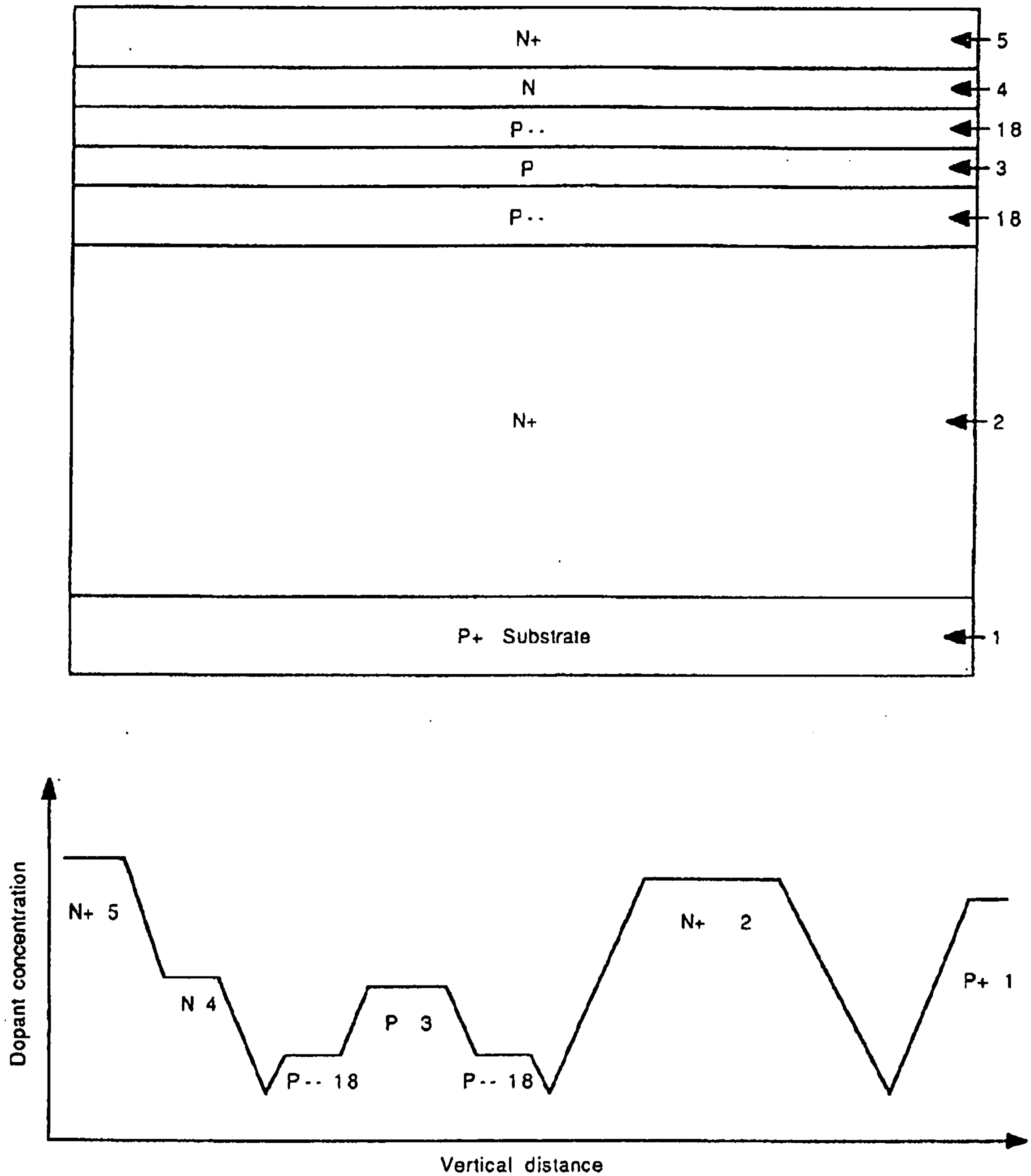
Dopant concentration
N+ 2
P+ 1
P- - 18
Vertical distance

Fig.1A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N 4
P-- 18
P 3
P-- 18
N+ 2
P+ 1
Vertical distance

Fig.1B

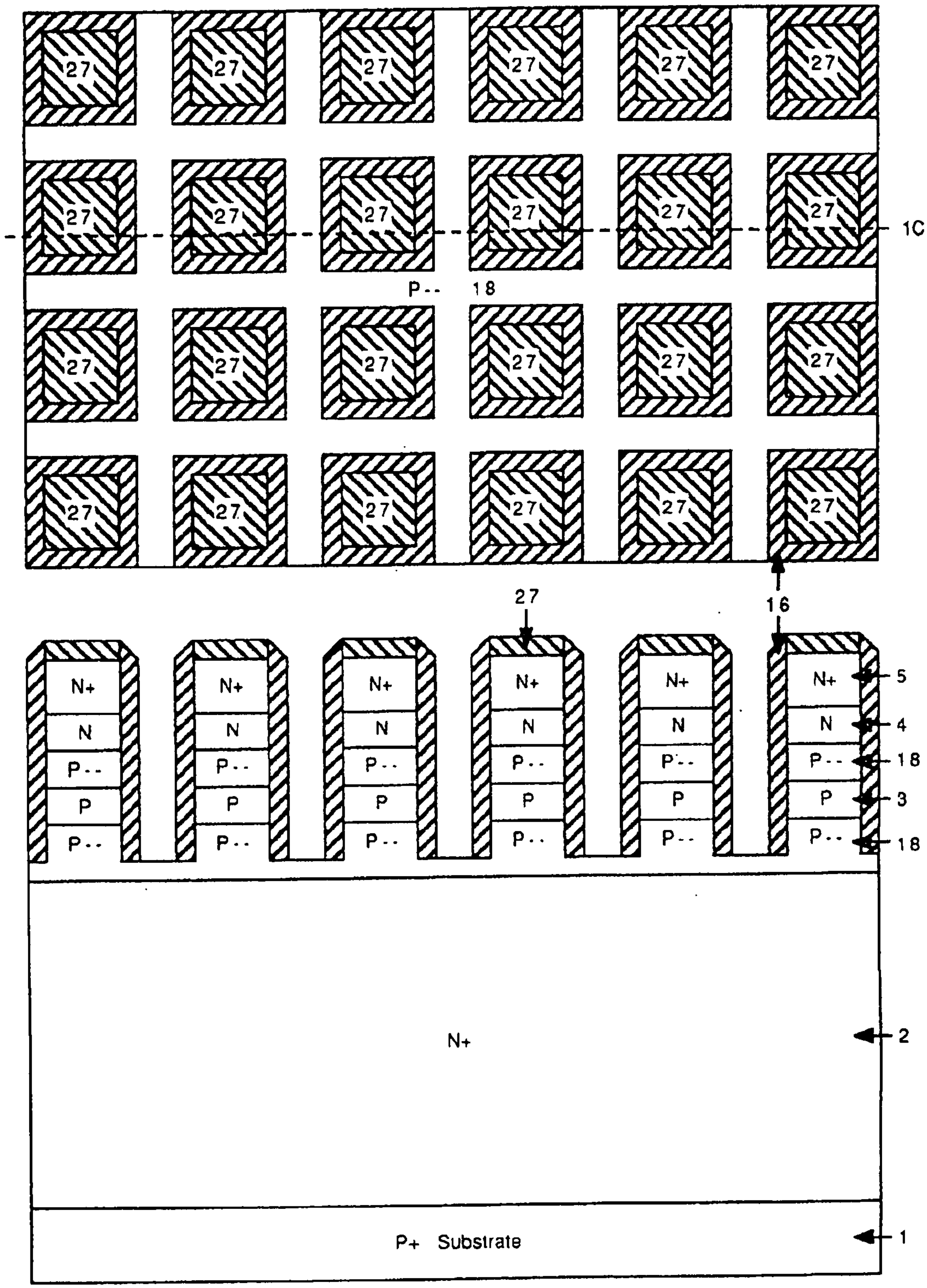


Fig.1C

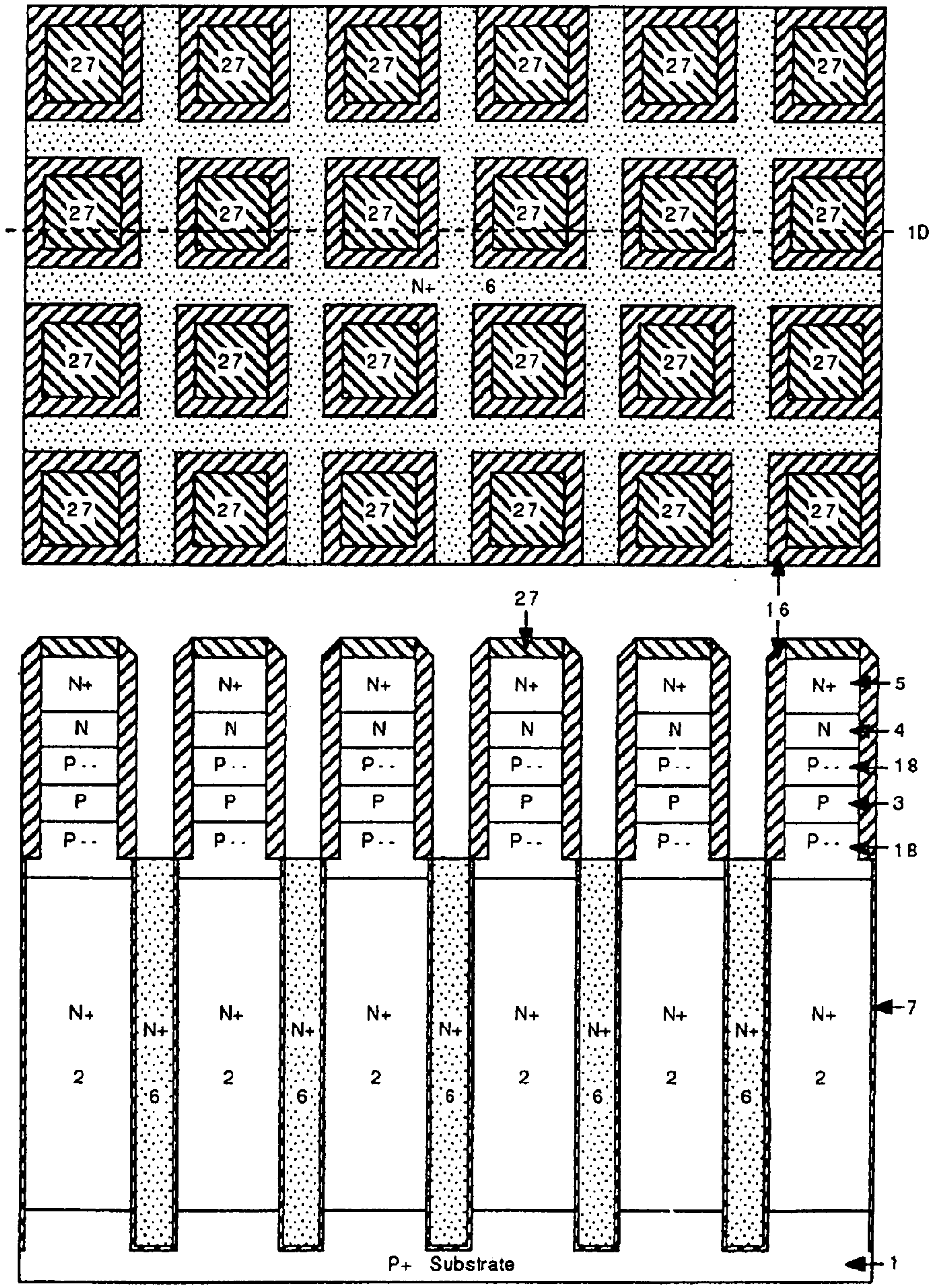


Fig.1D

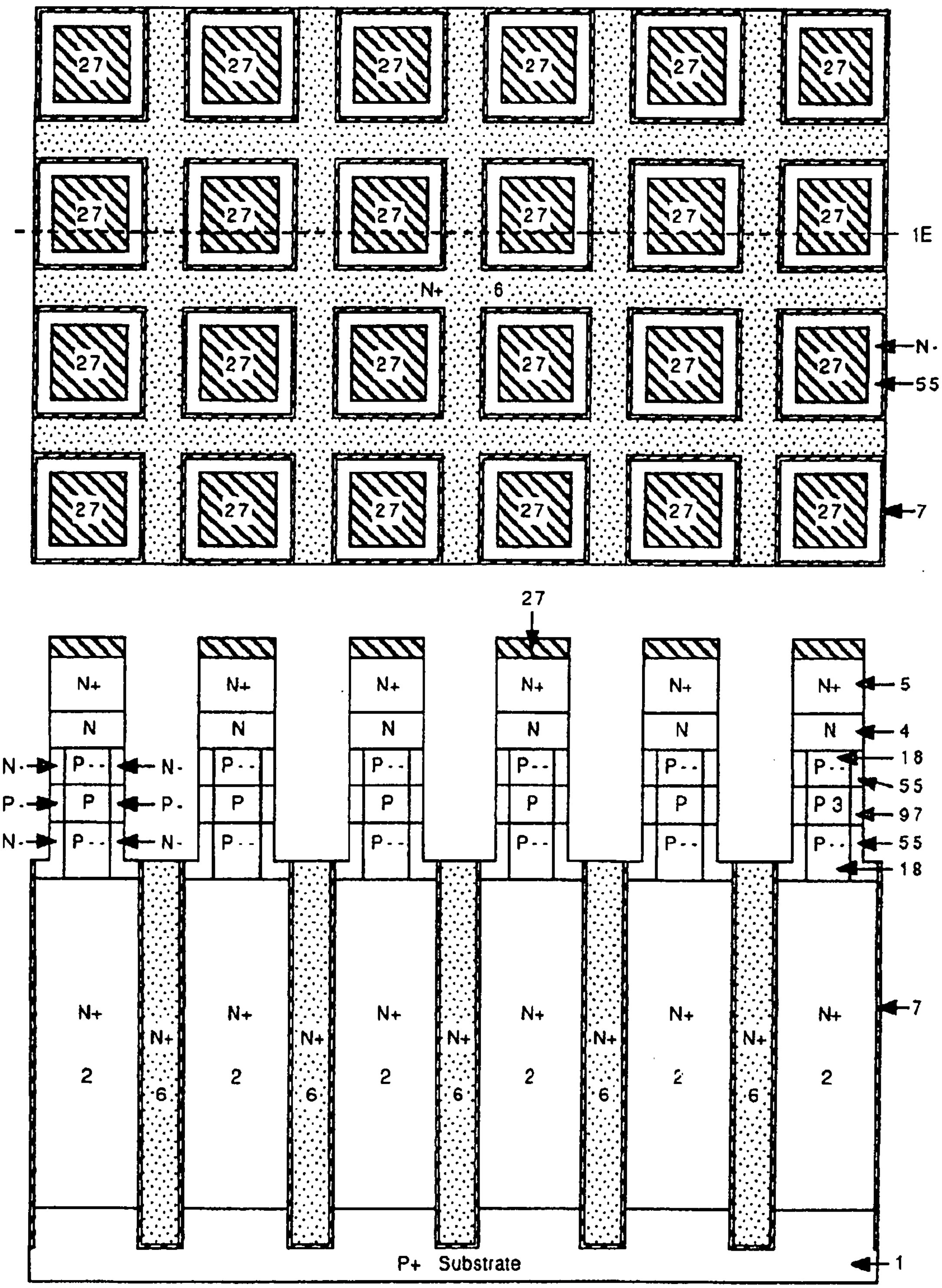
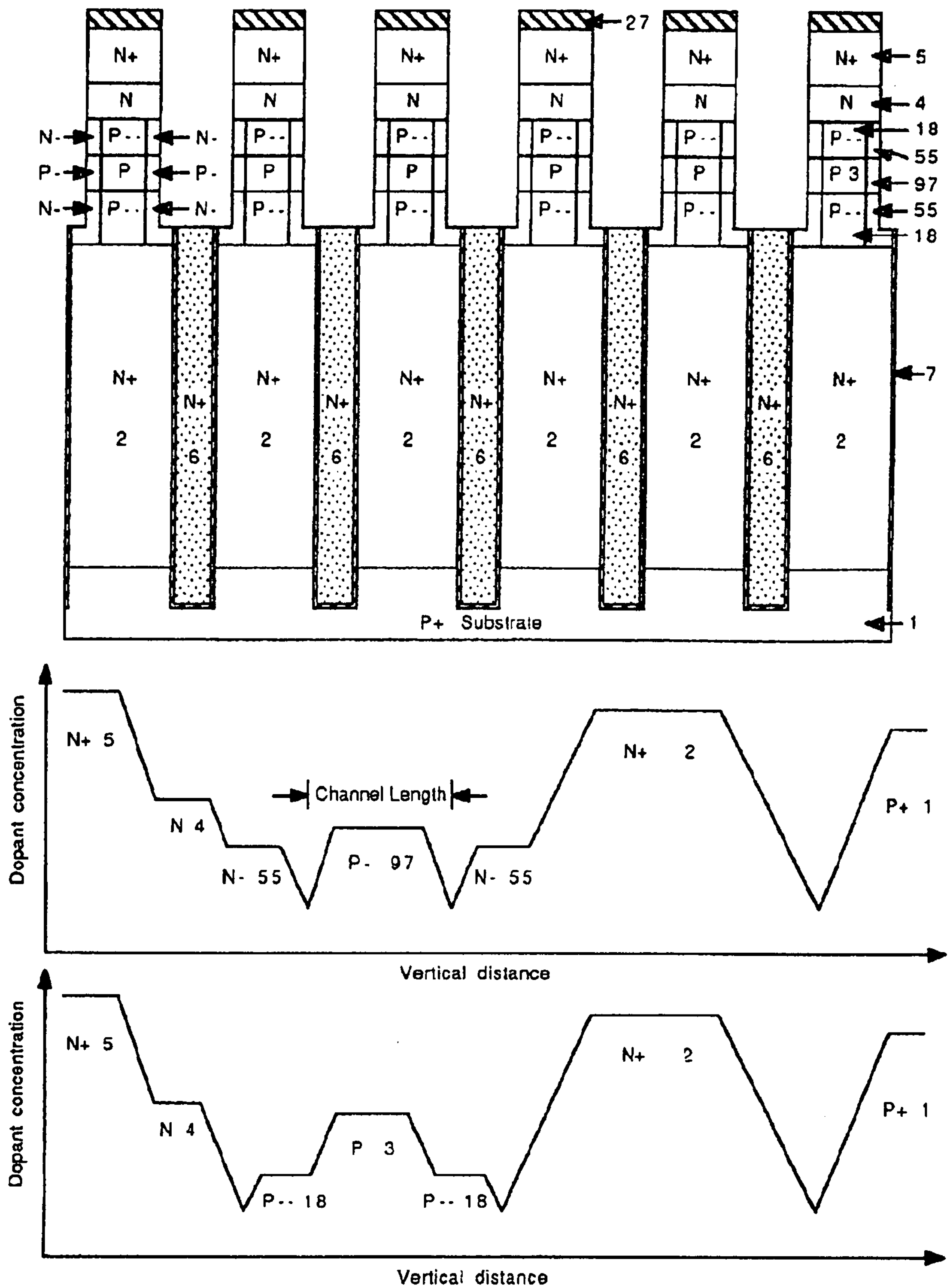


Fig.1E



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6
7
P+ Substrate
1
Dopant concentration
N+ 5
N 4
N- 55
Channel Length
P- 97
N- 55
N+ 2
P+ 1
Vertical distance
Dopant concentration
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N 4
P-- 18
P 3
P-- 18
N+ 2
P+ 1
Vertical distance

Fig.1E1

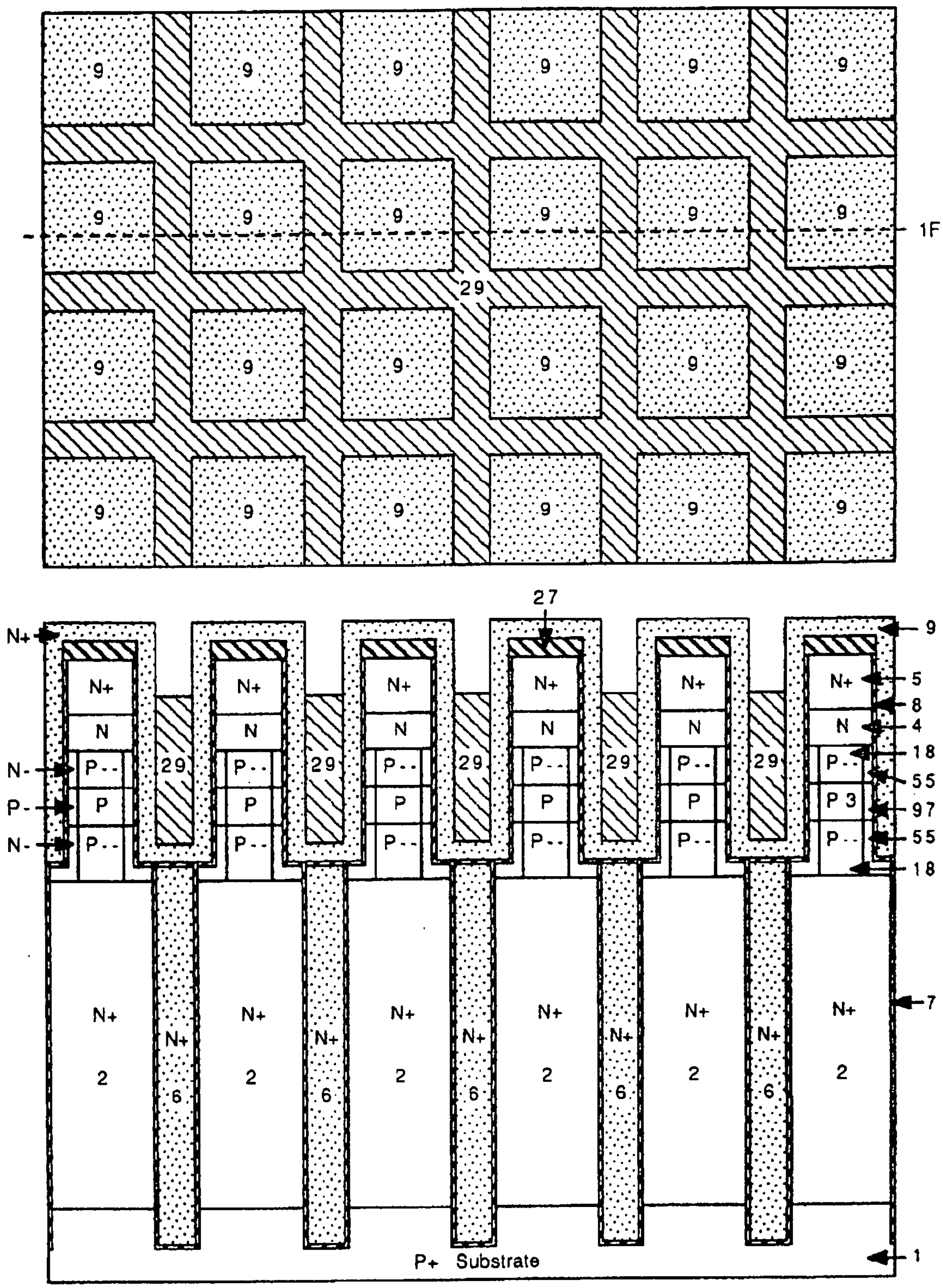


Fig.1F

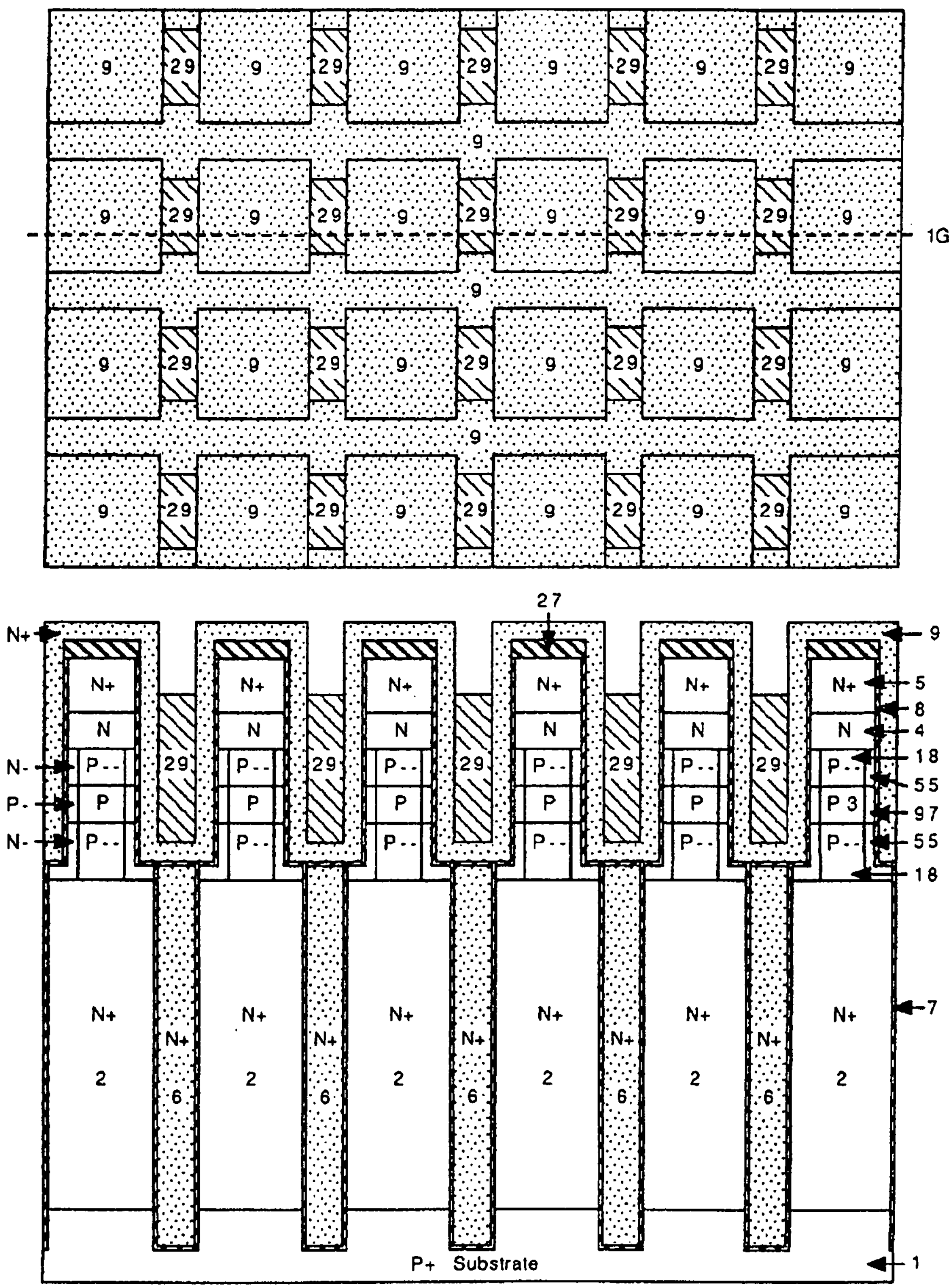


Fig.1G

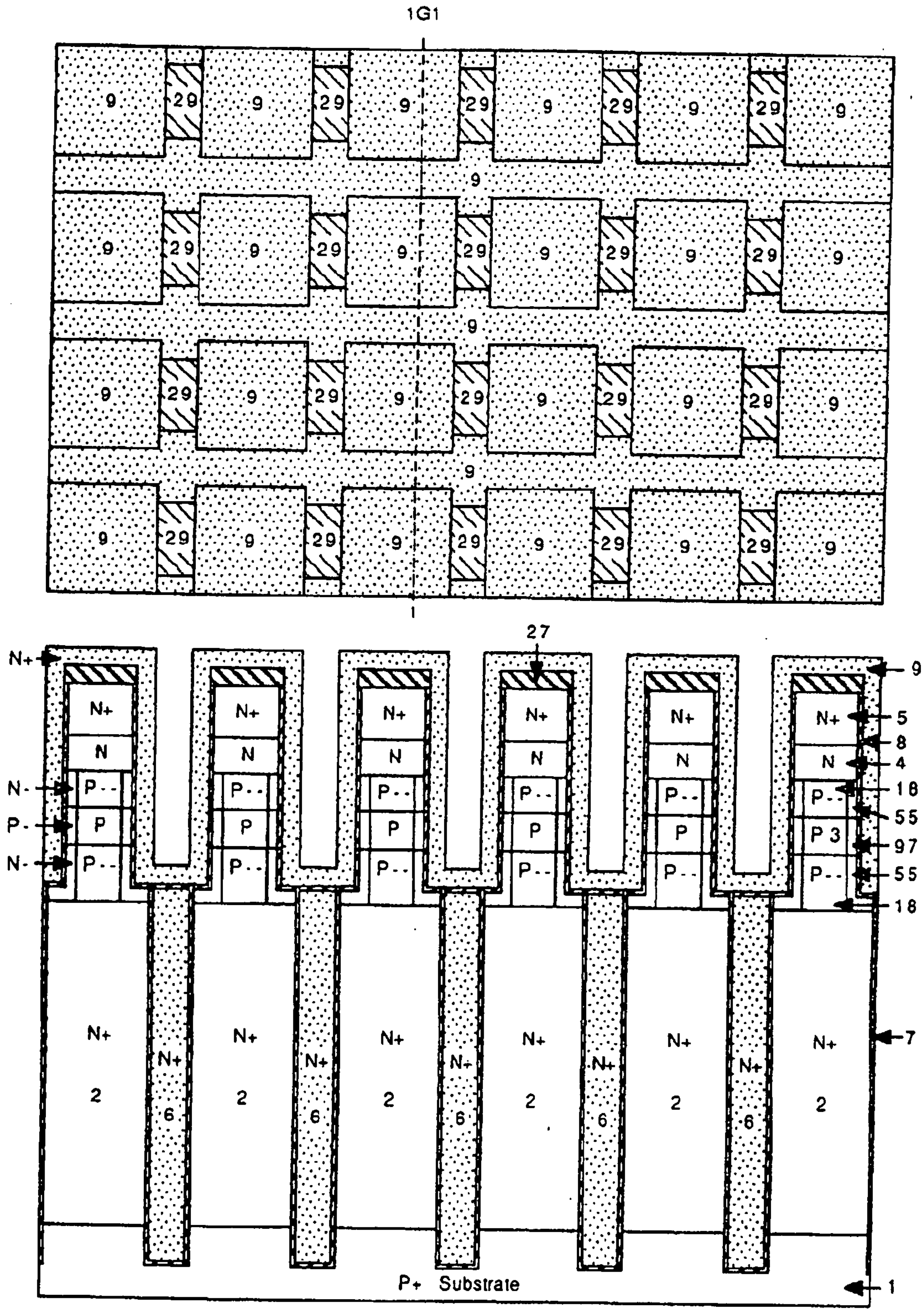


Fig.1G1

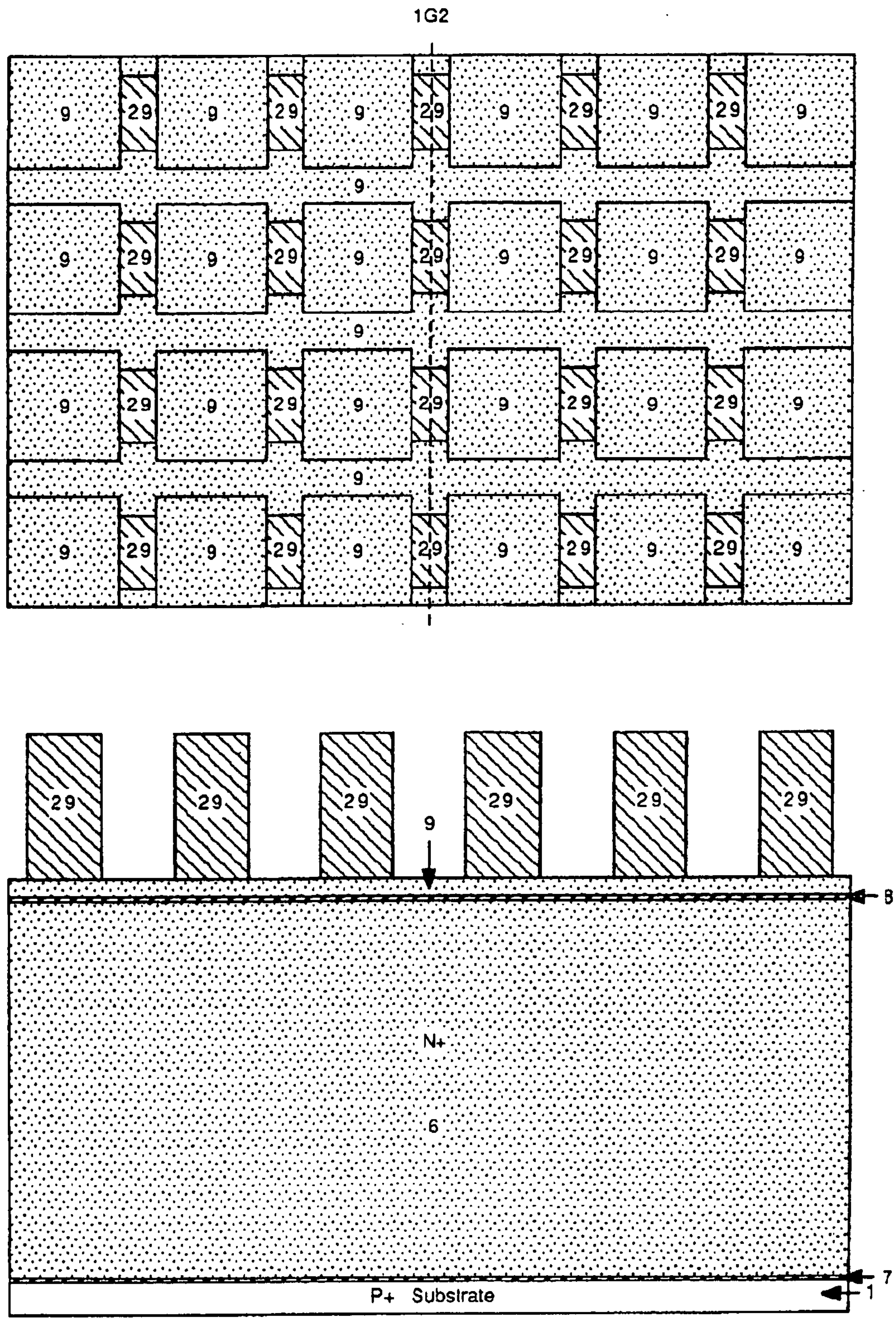


Fig.1G2

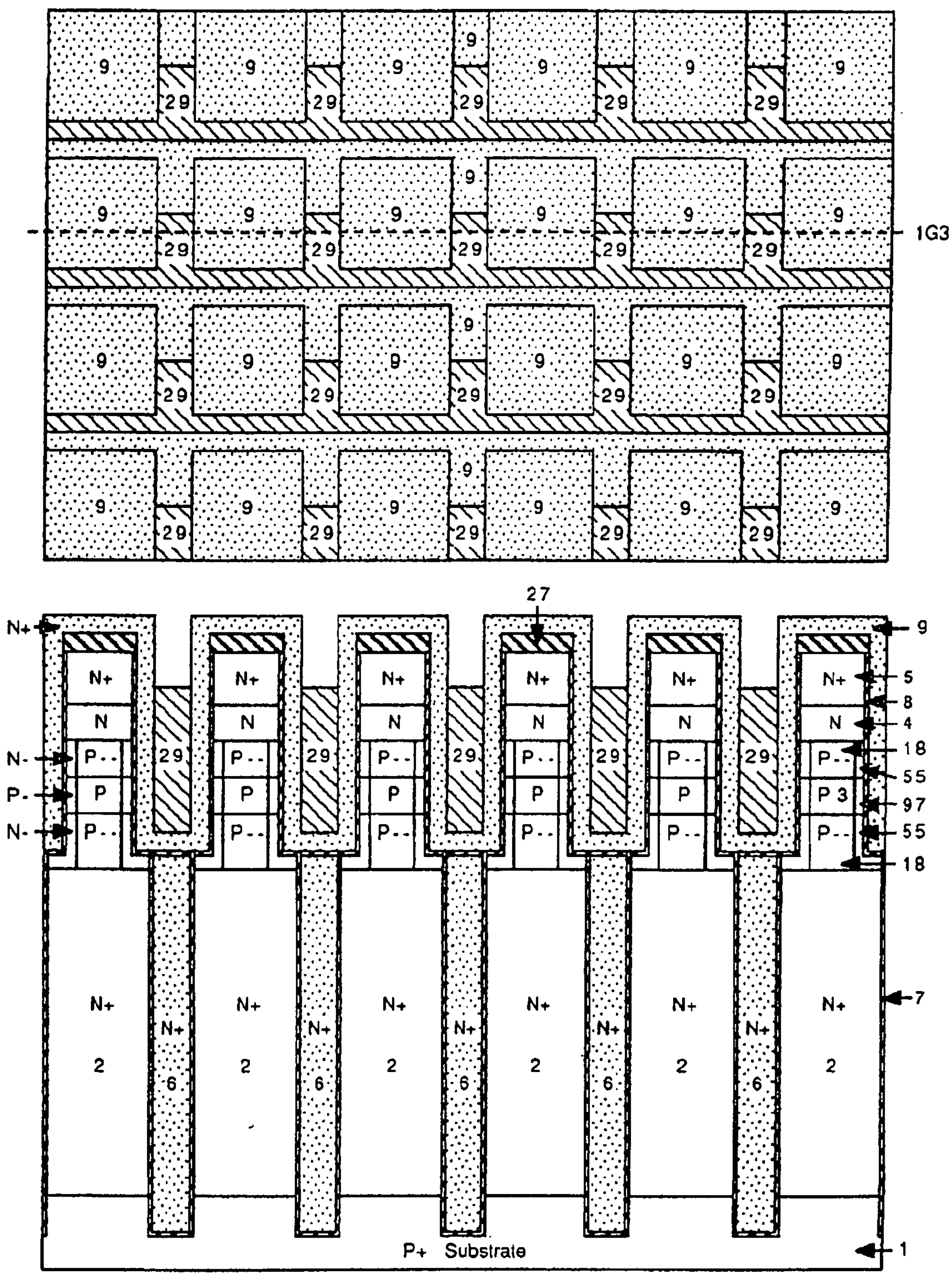


Fig.1G3

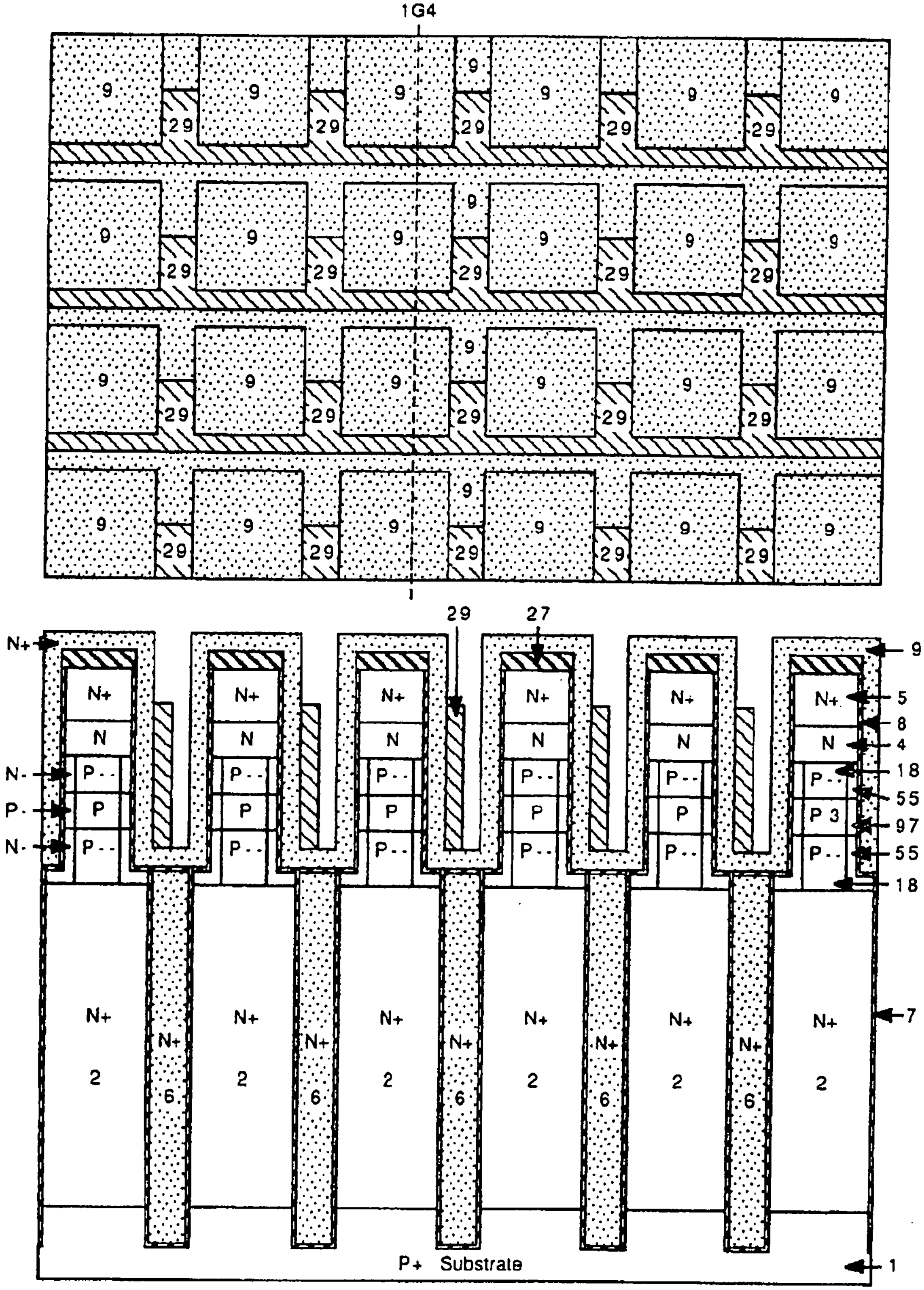


Fig.1G4

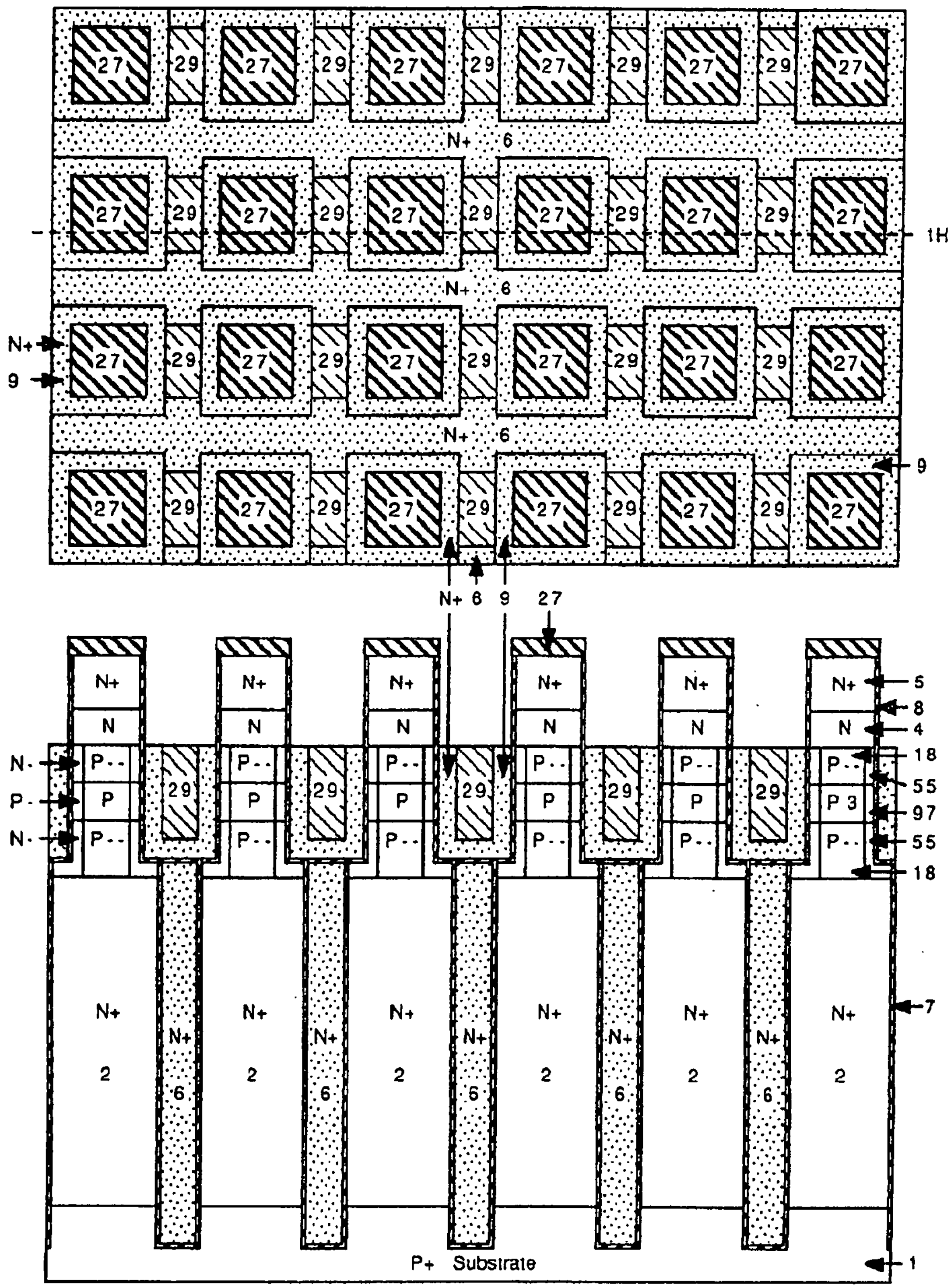


Fig.1H

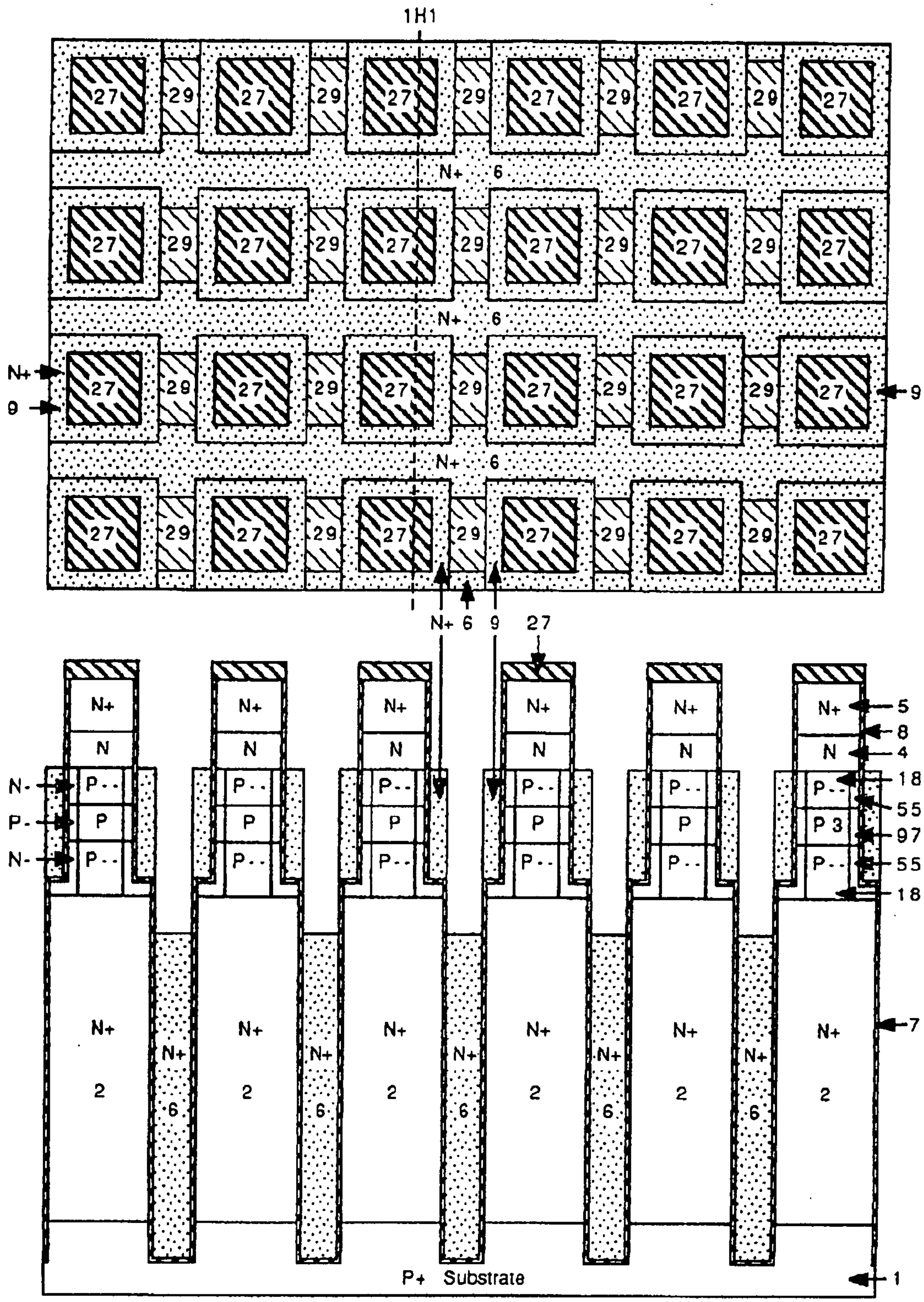
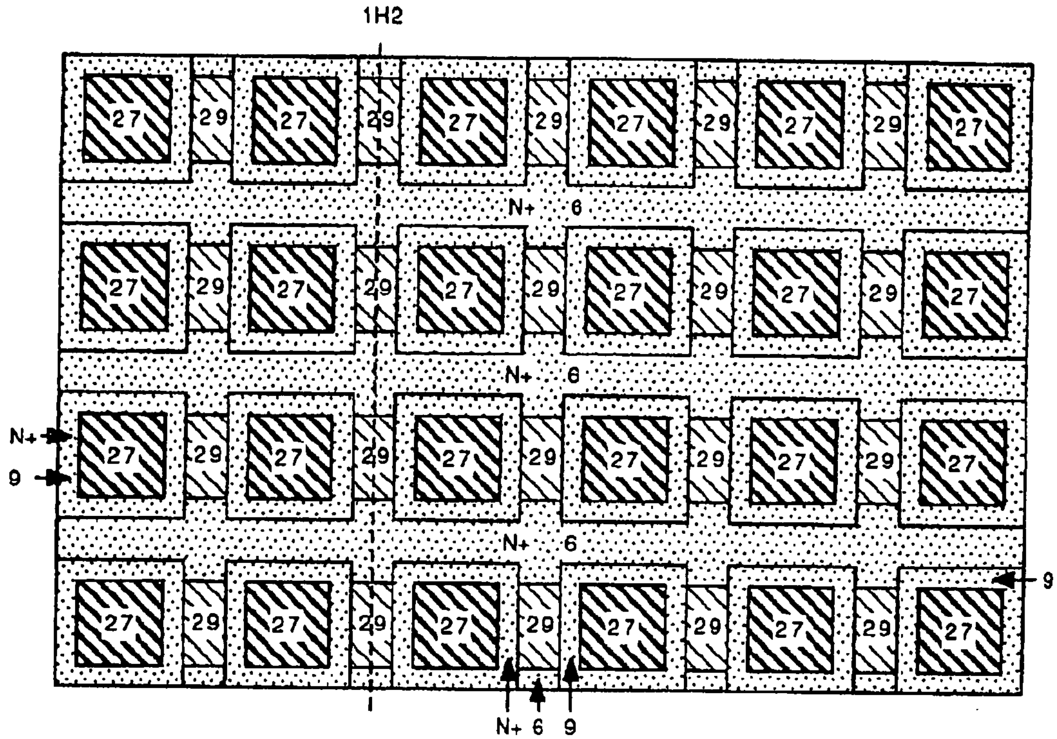


Fig.1H1



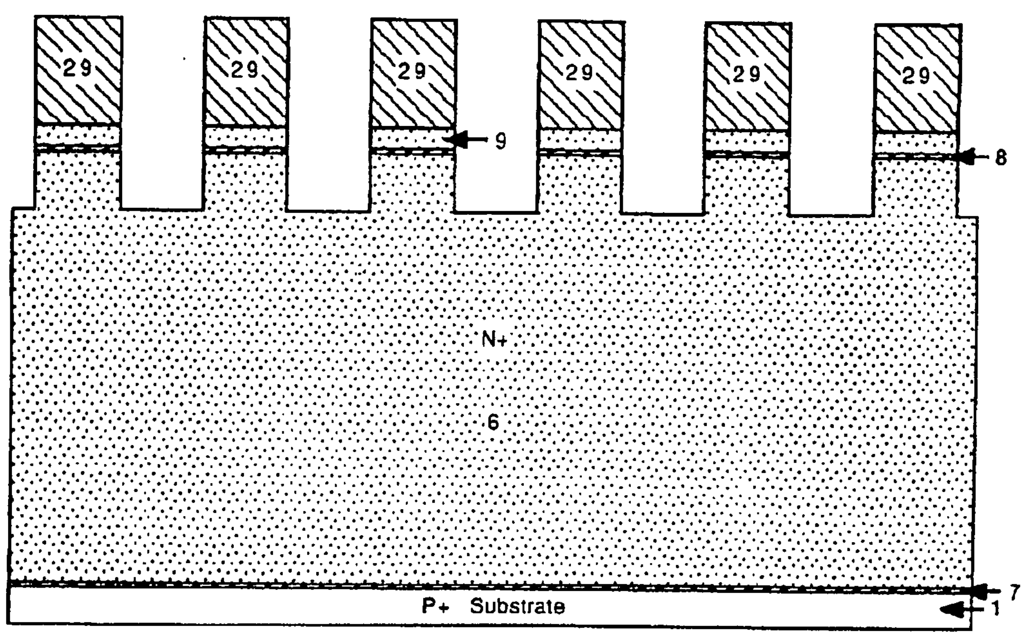


Fig.1H2

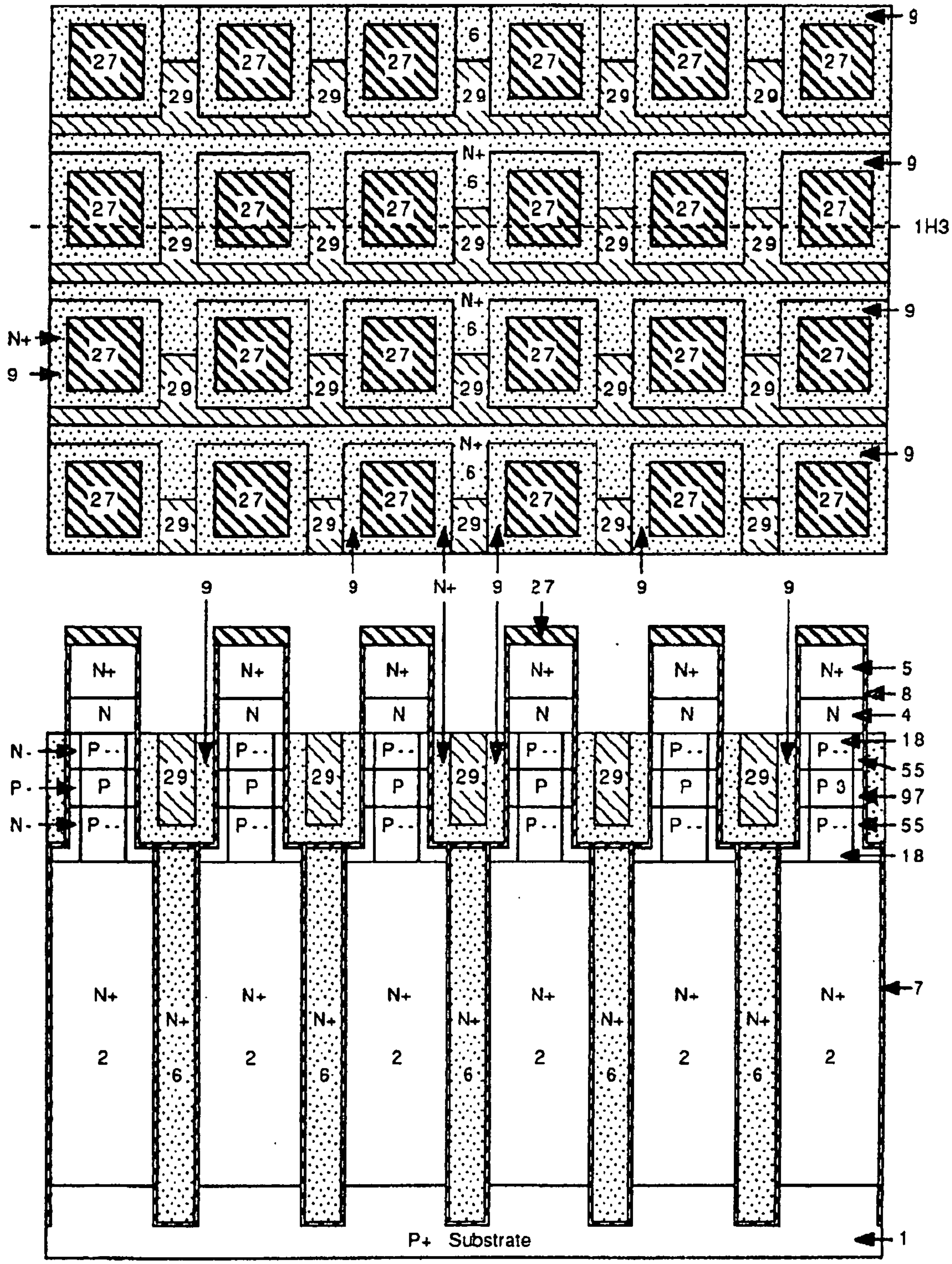


Fig.1H3

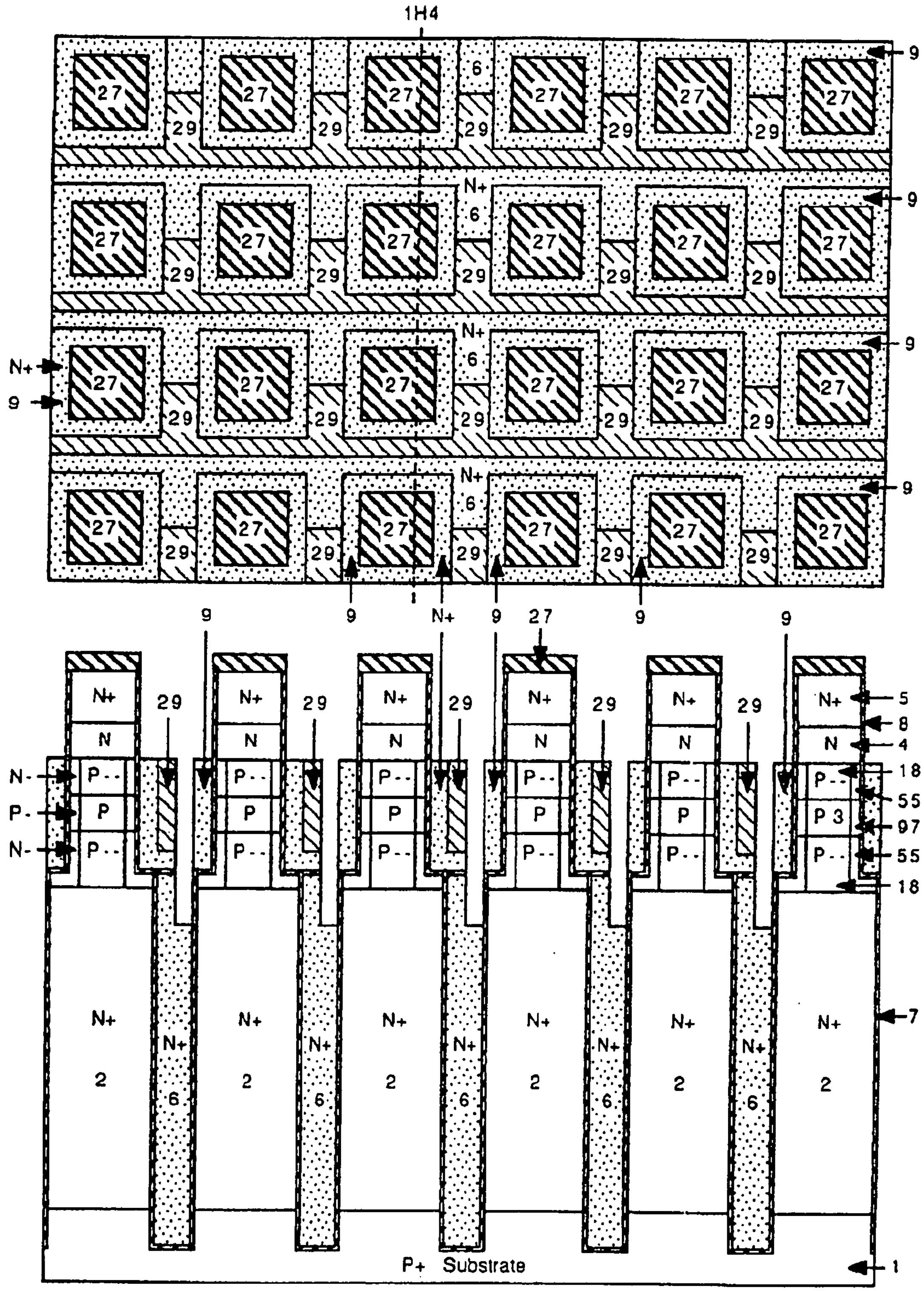
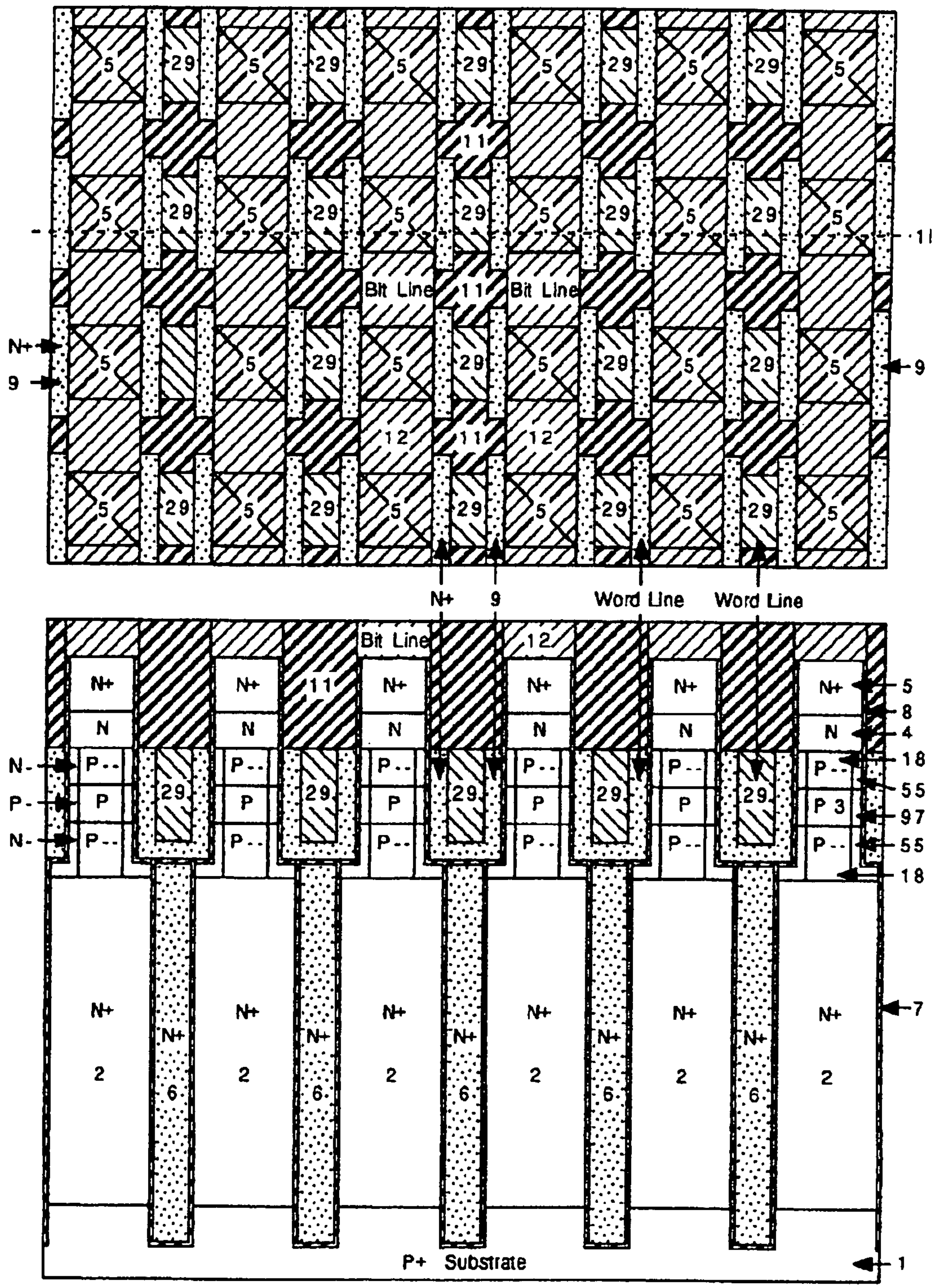


Fig.1H4



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P+ Substrate
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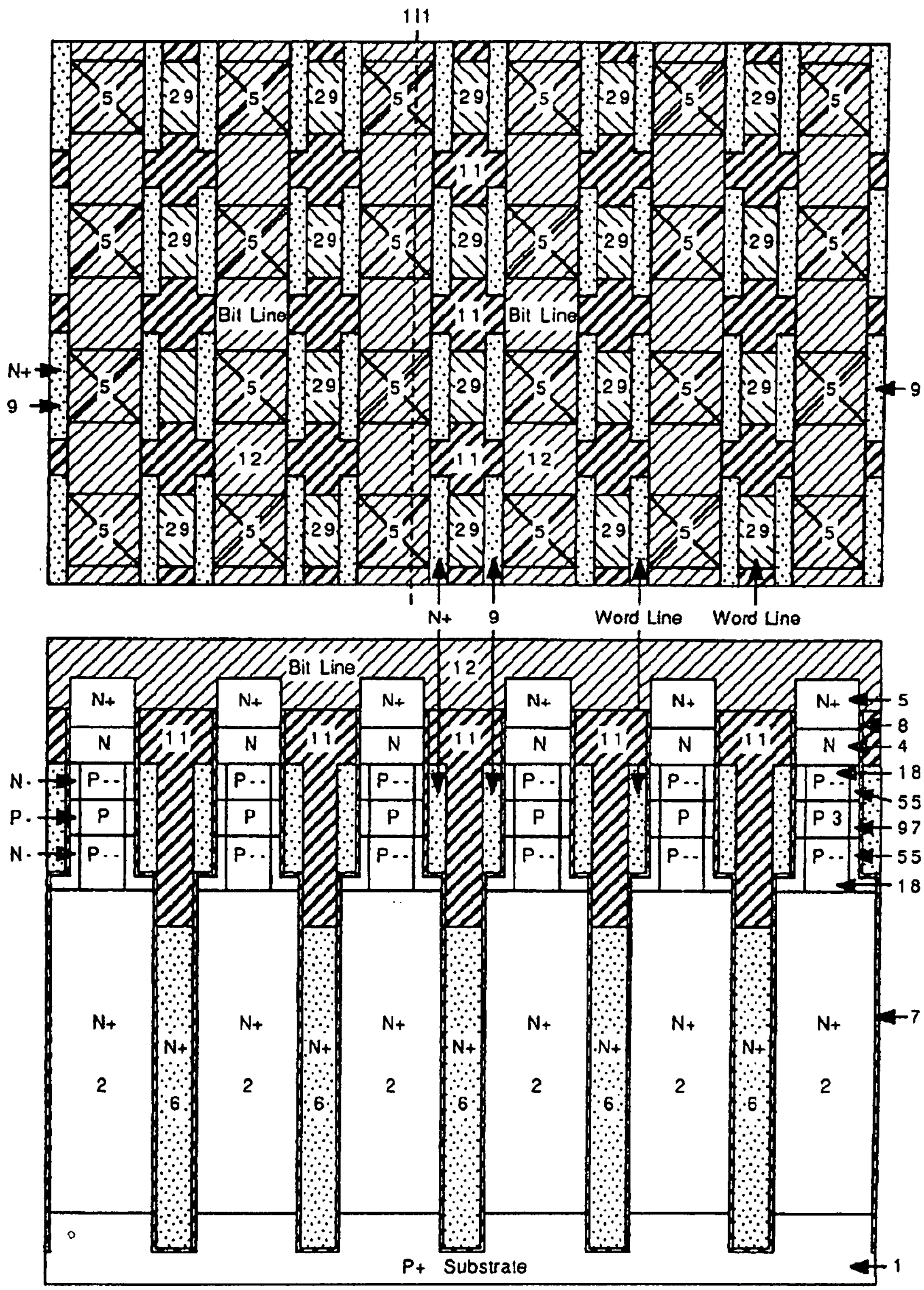
Fig.1l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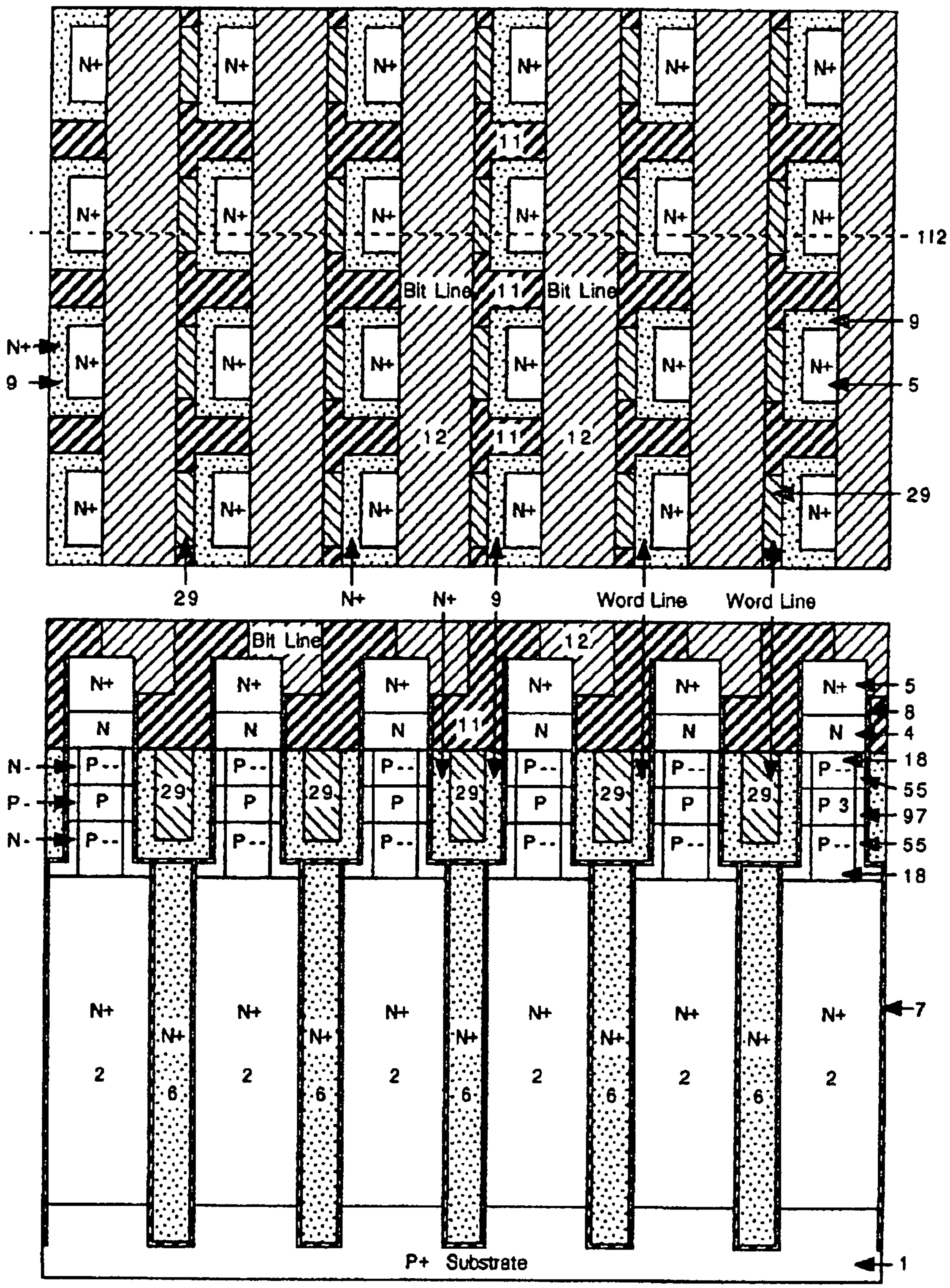
P+ Substrate

Fig.1l1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P+ Substrate
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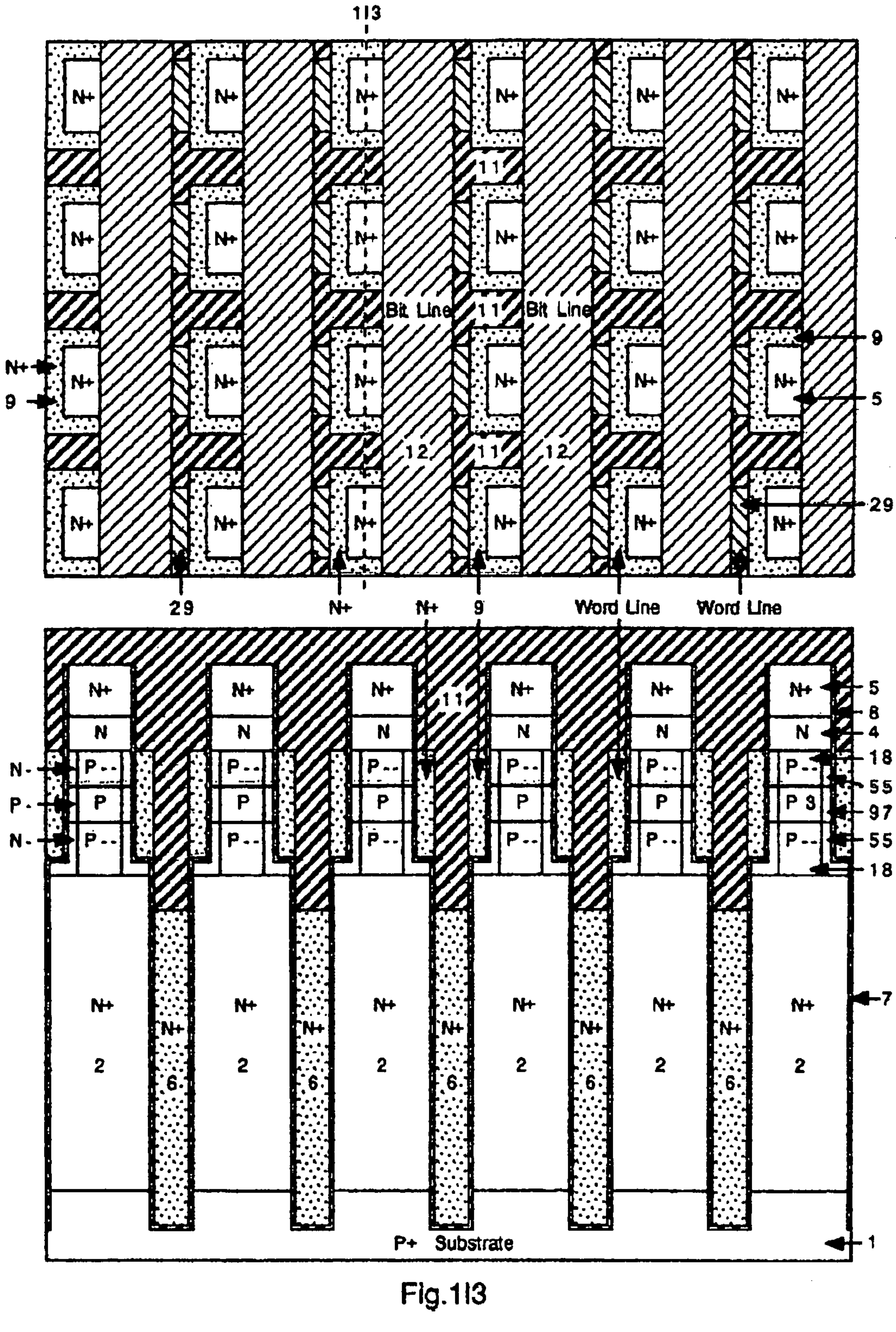
Fig.112



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P+ Substrate

Fig.113

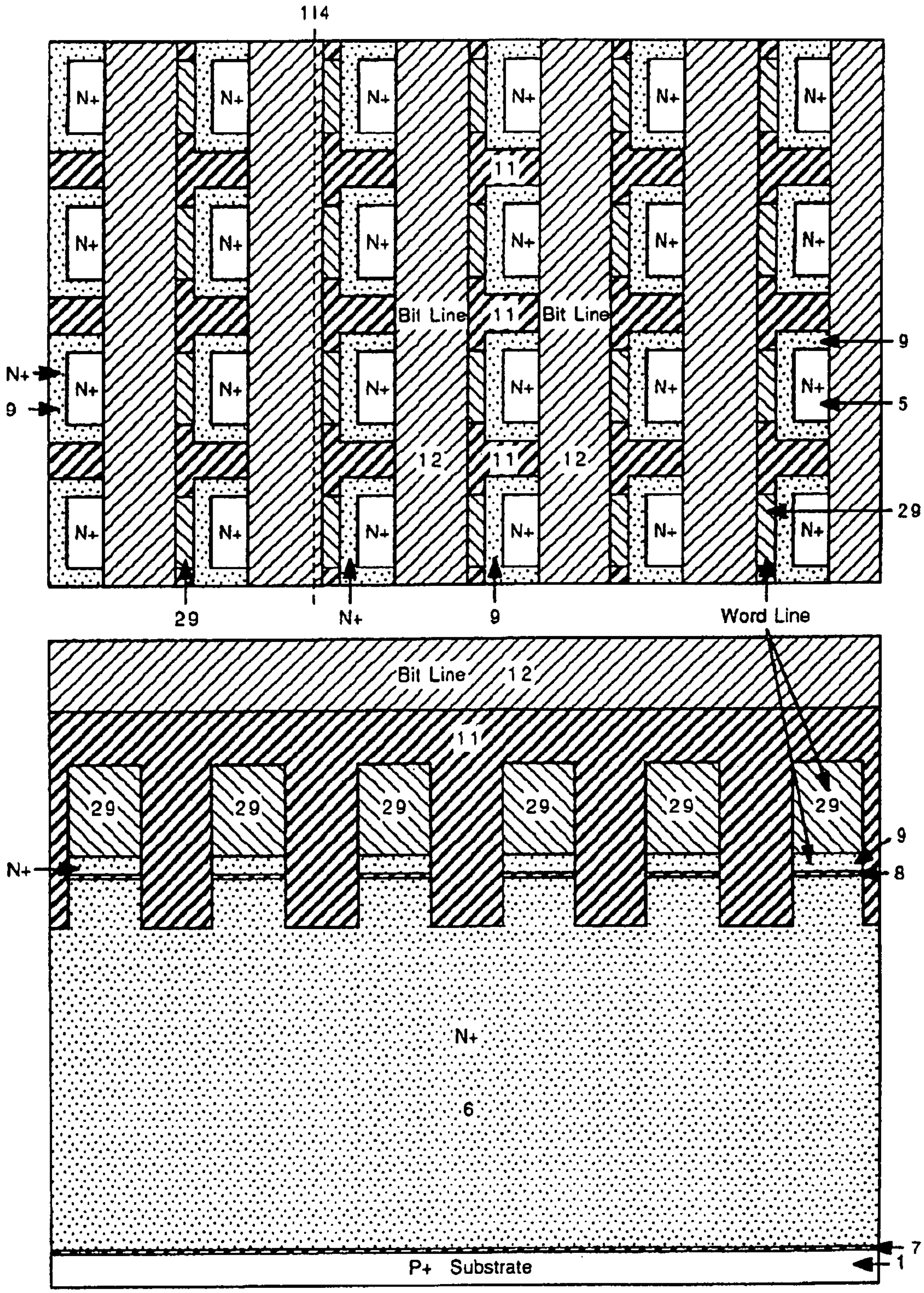
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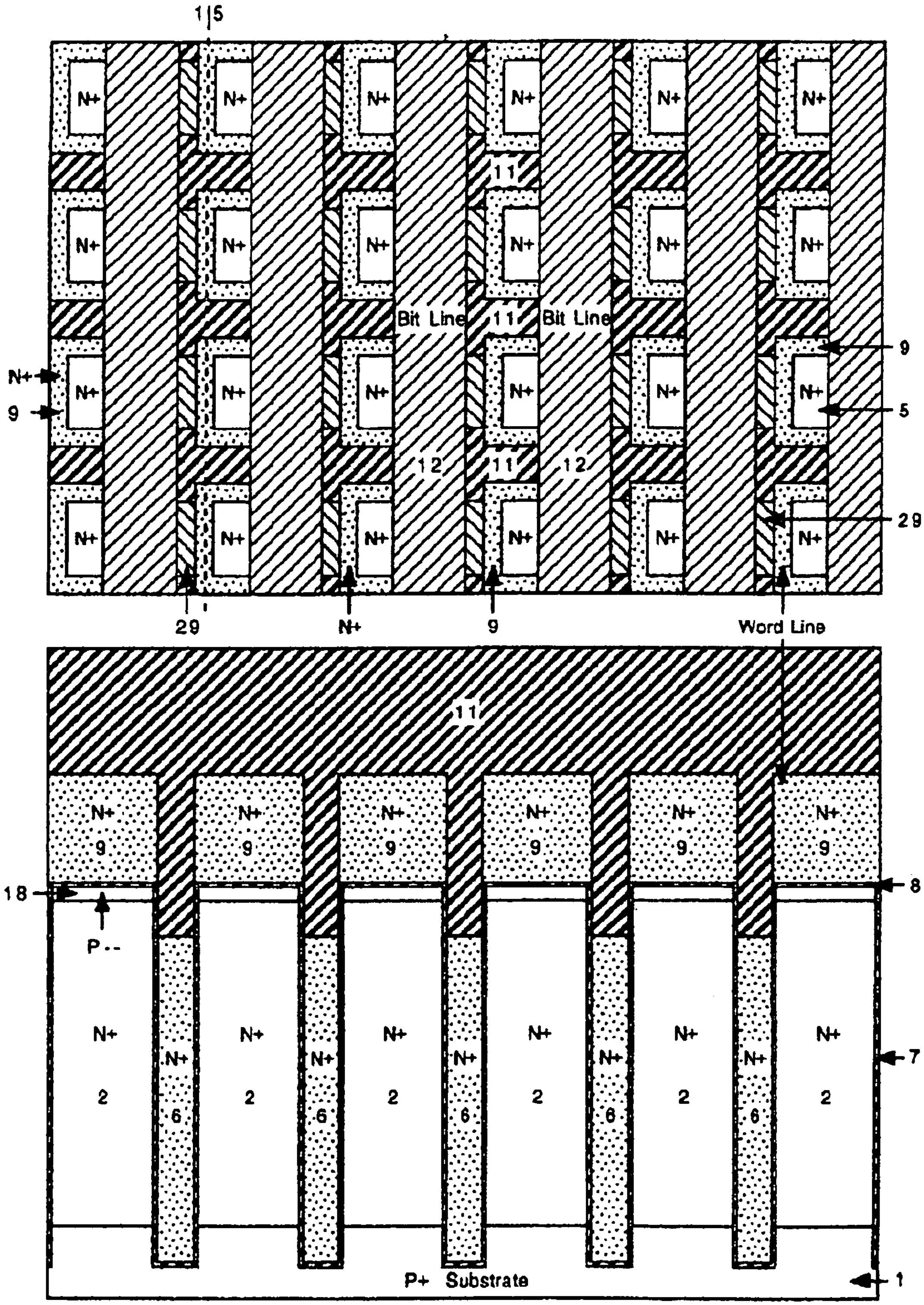
Fig.114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P+ Substrate
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Fig.115

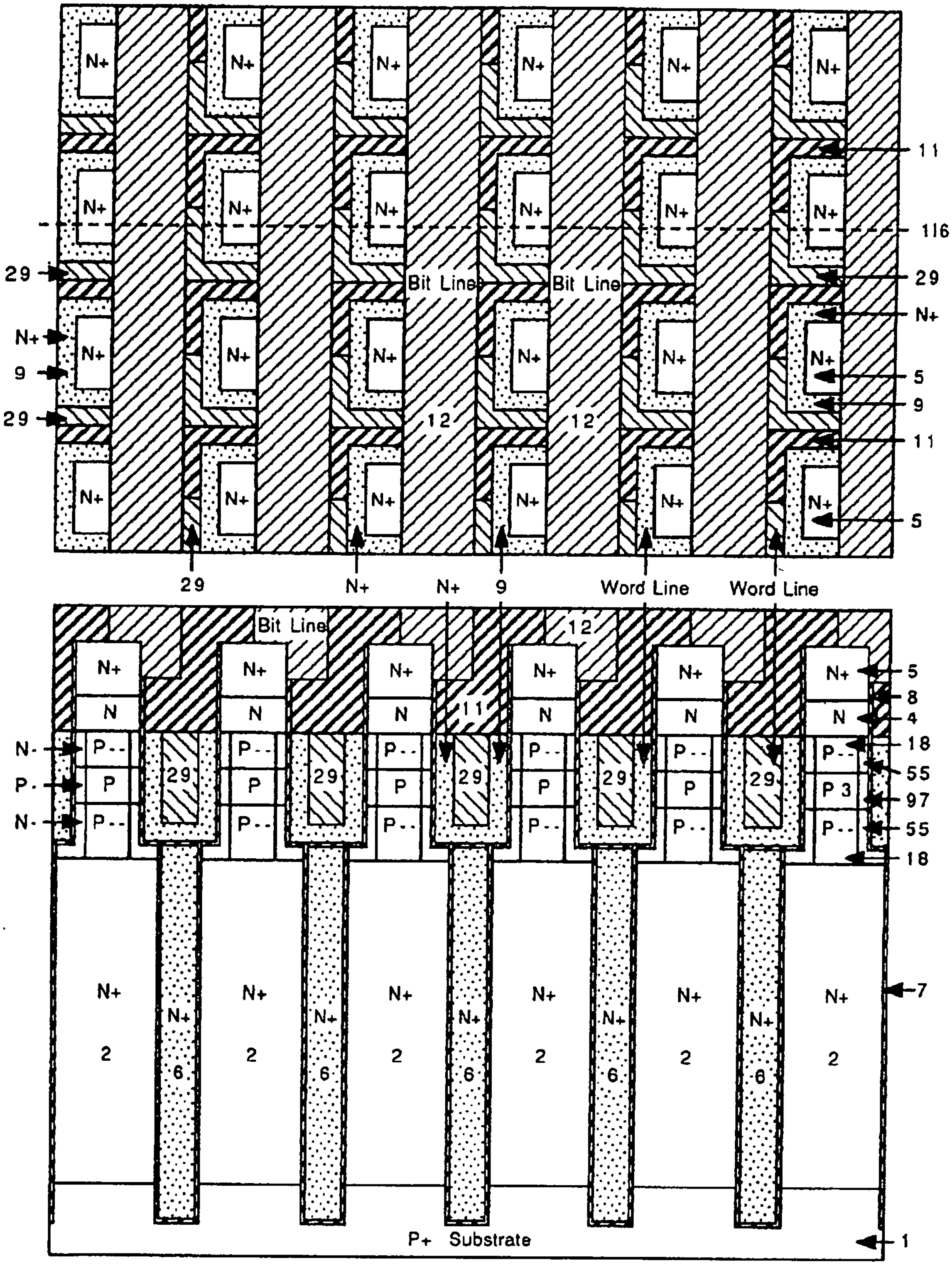
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Fig.116

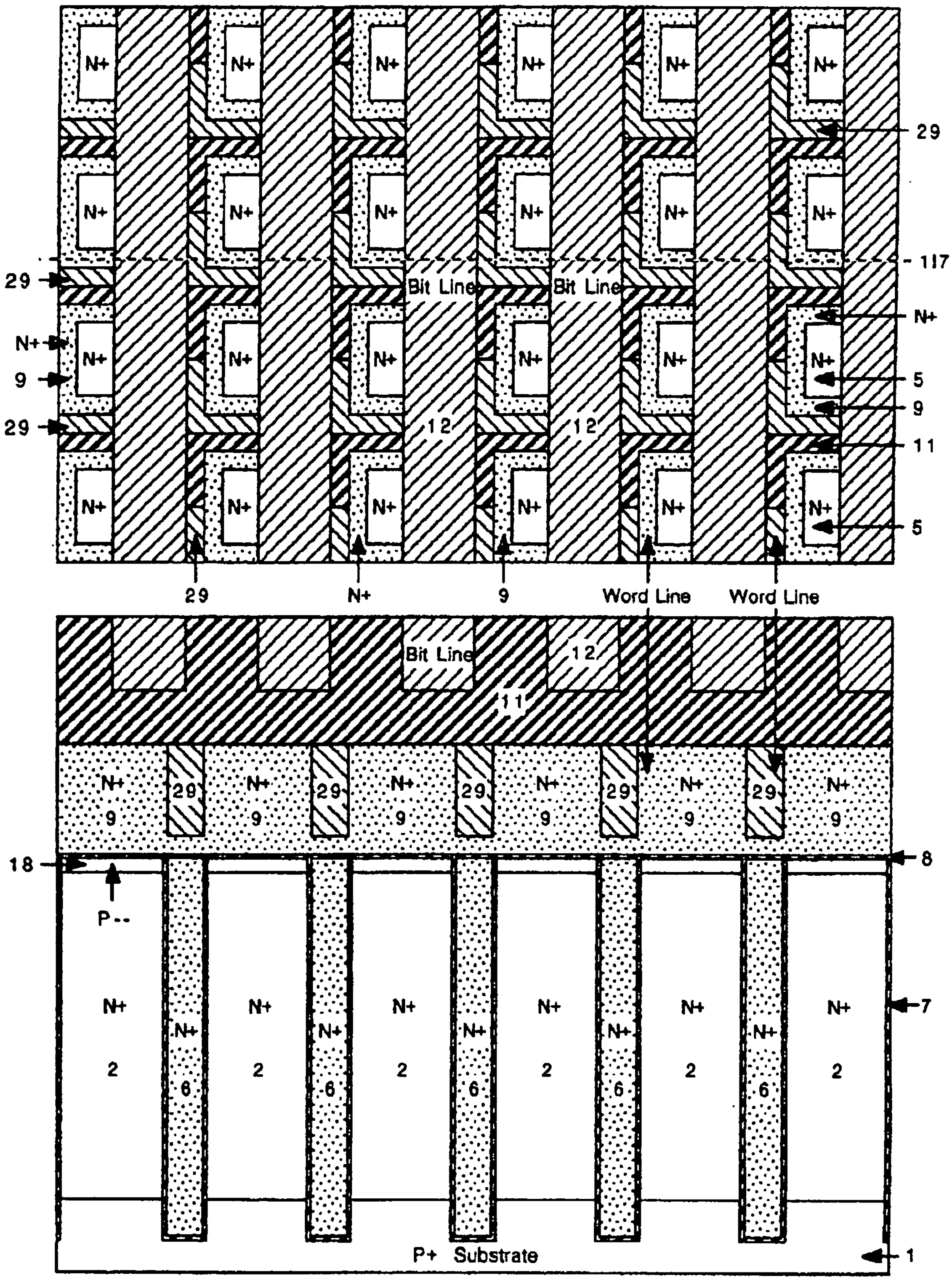

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Fig.117

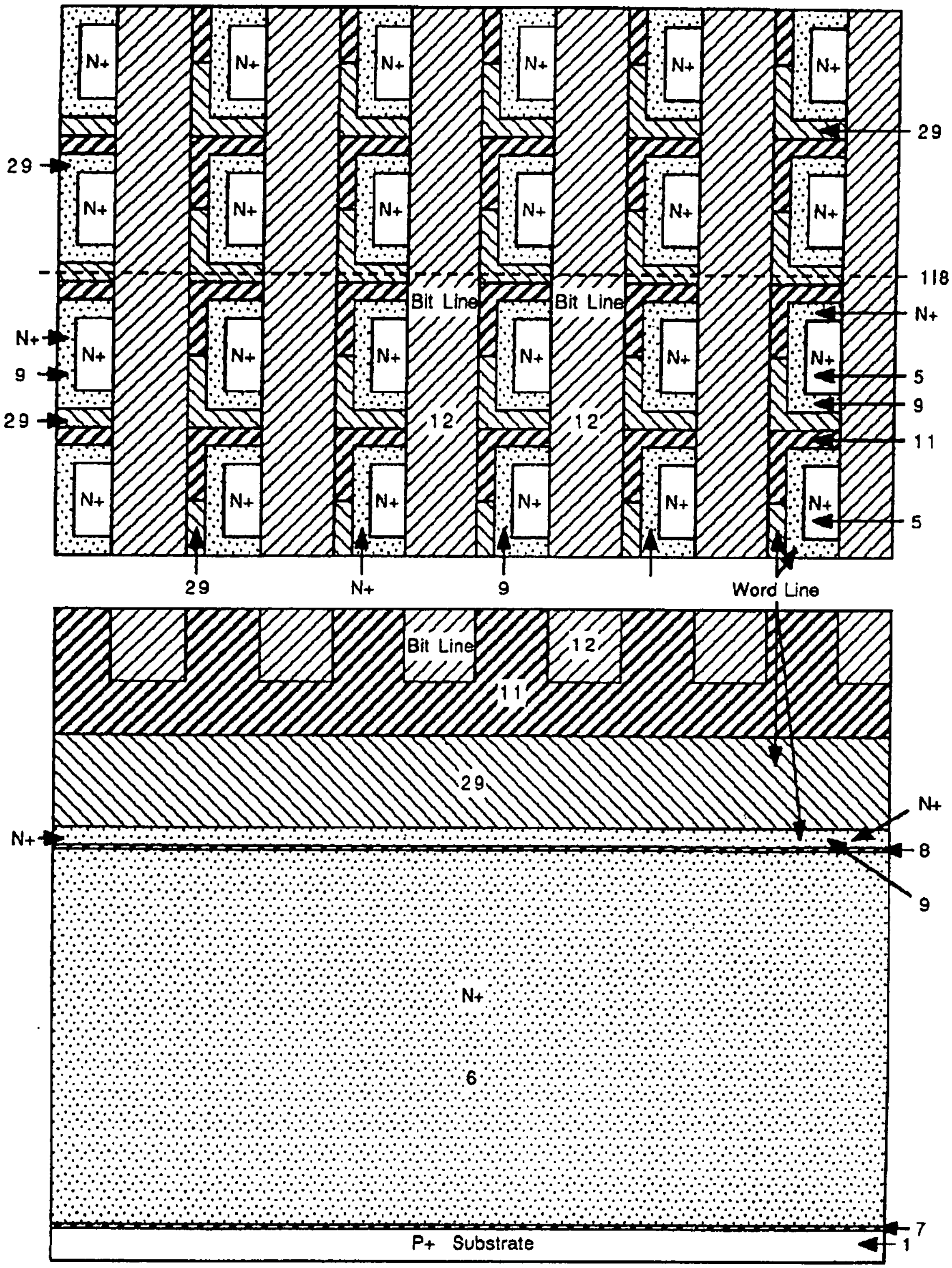
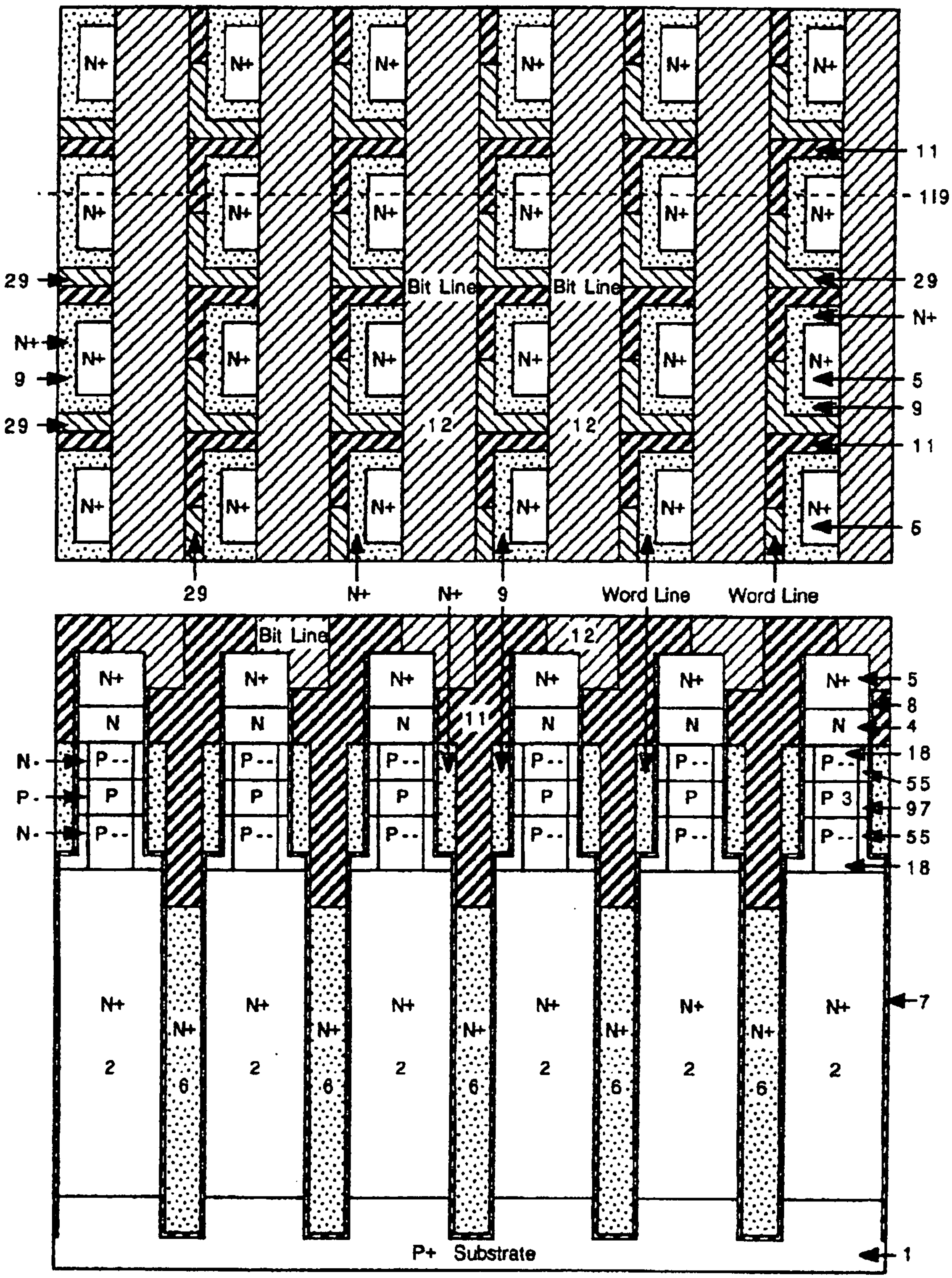


Fig.118



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P+ Substrate

Fig.119

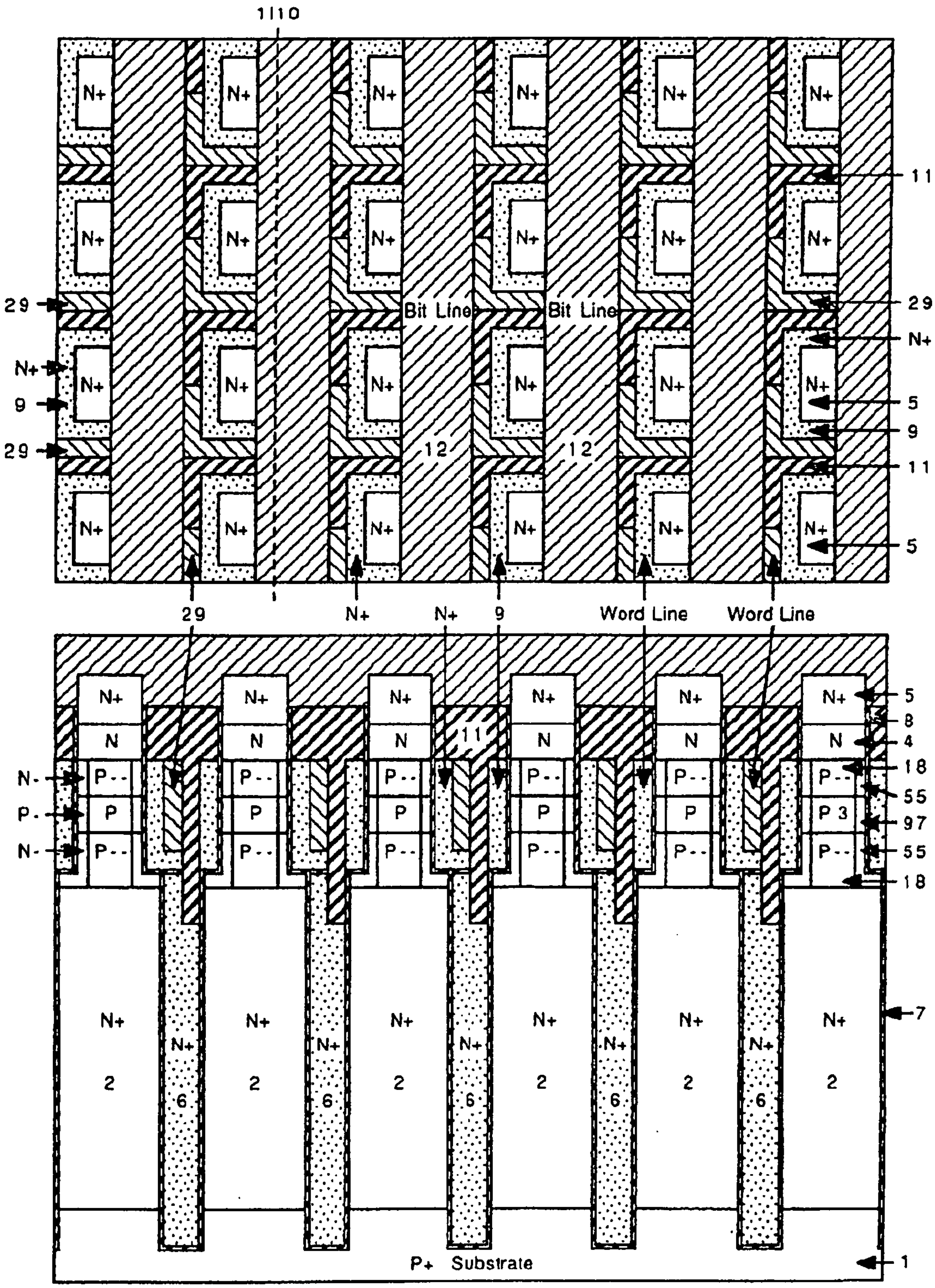
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Fig.1110

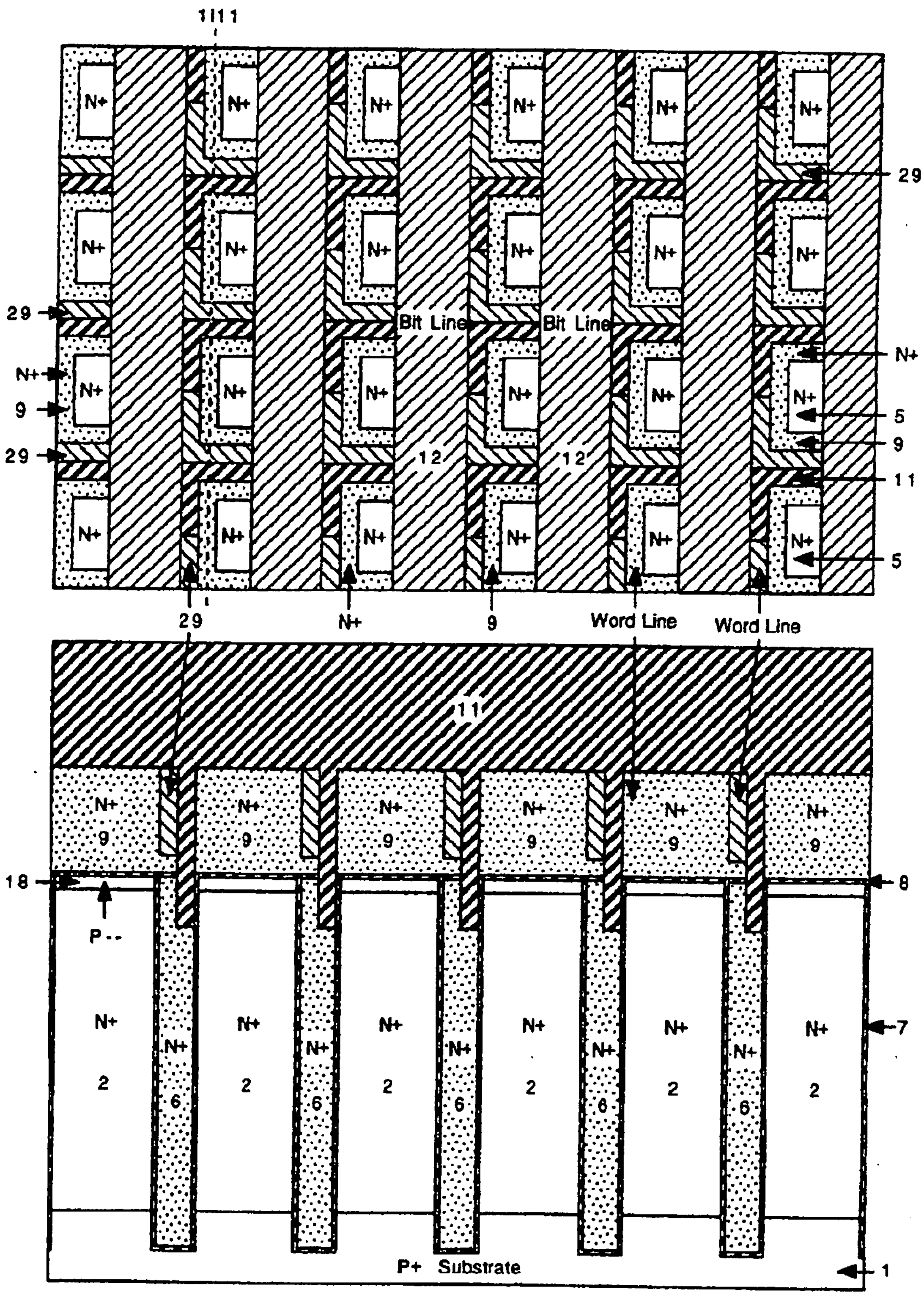

Fig.1I11

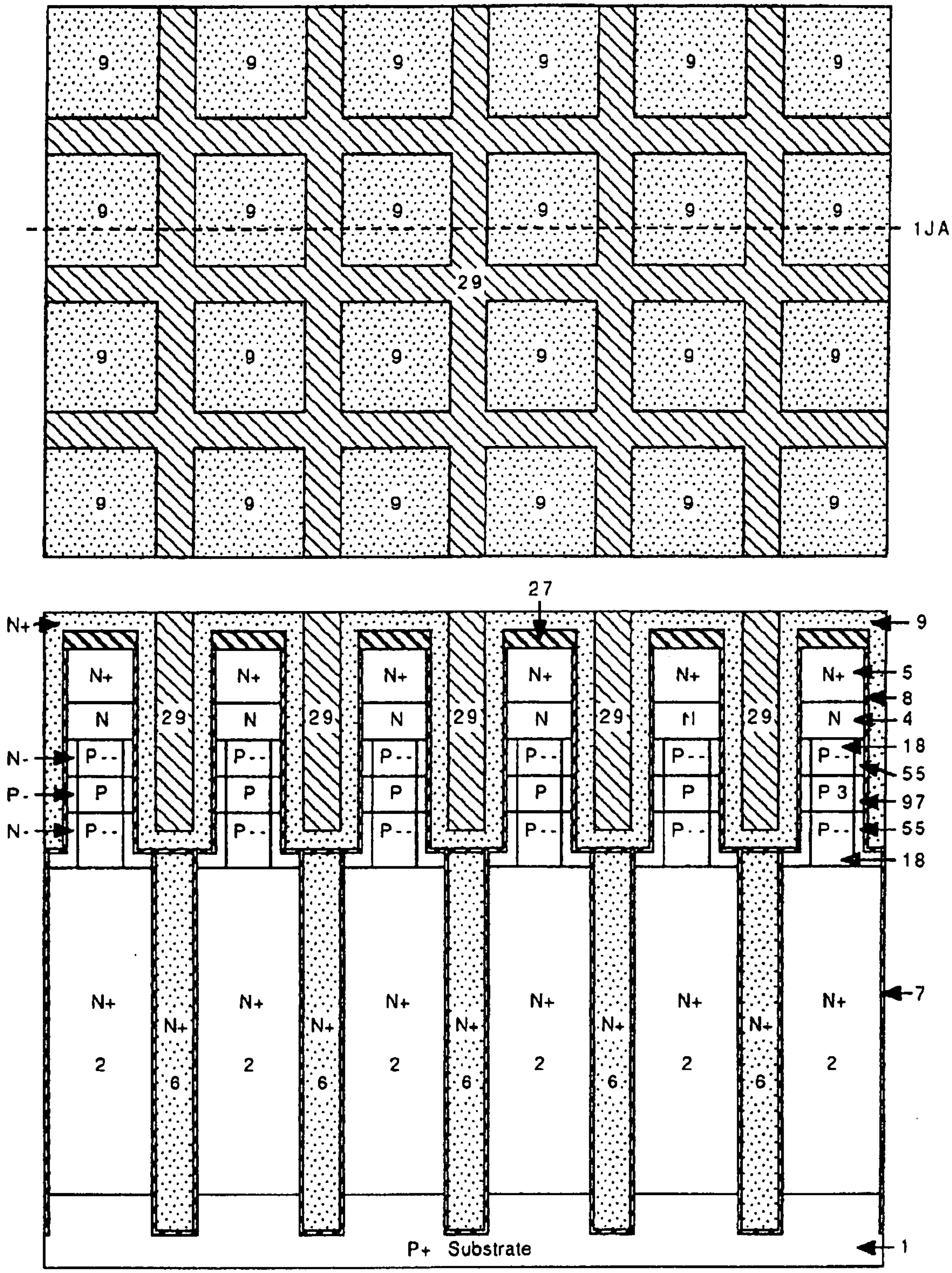

Fig.1JA

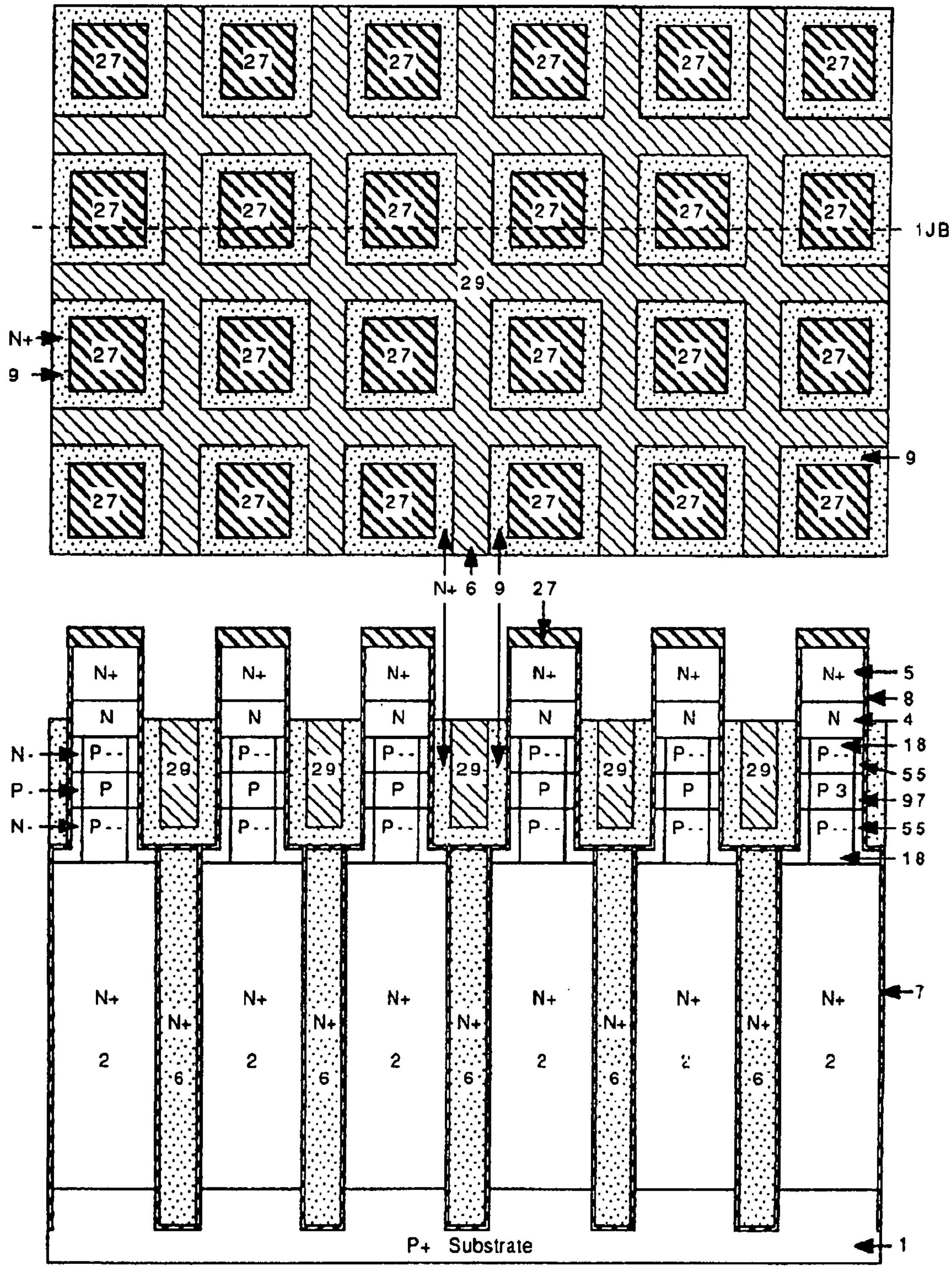
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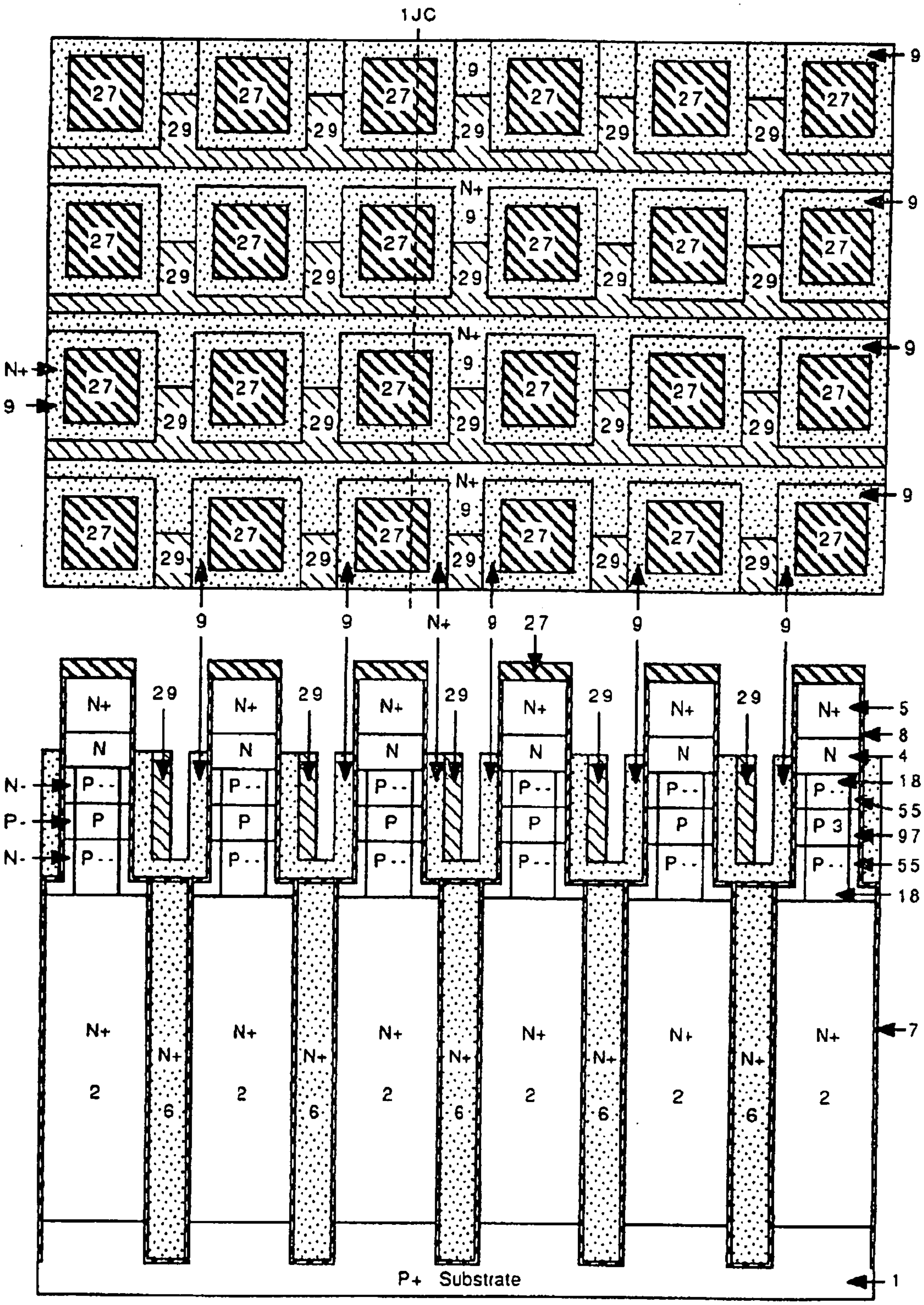
Fig.1JB



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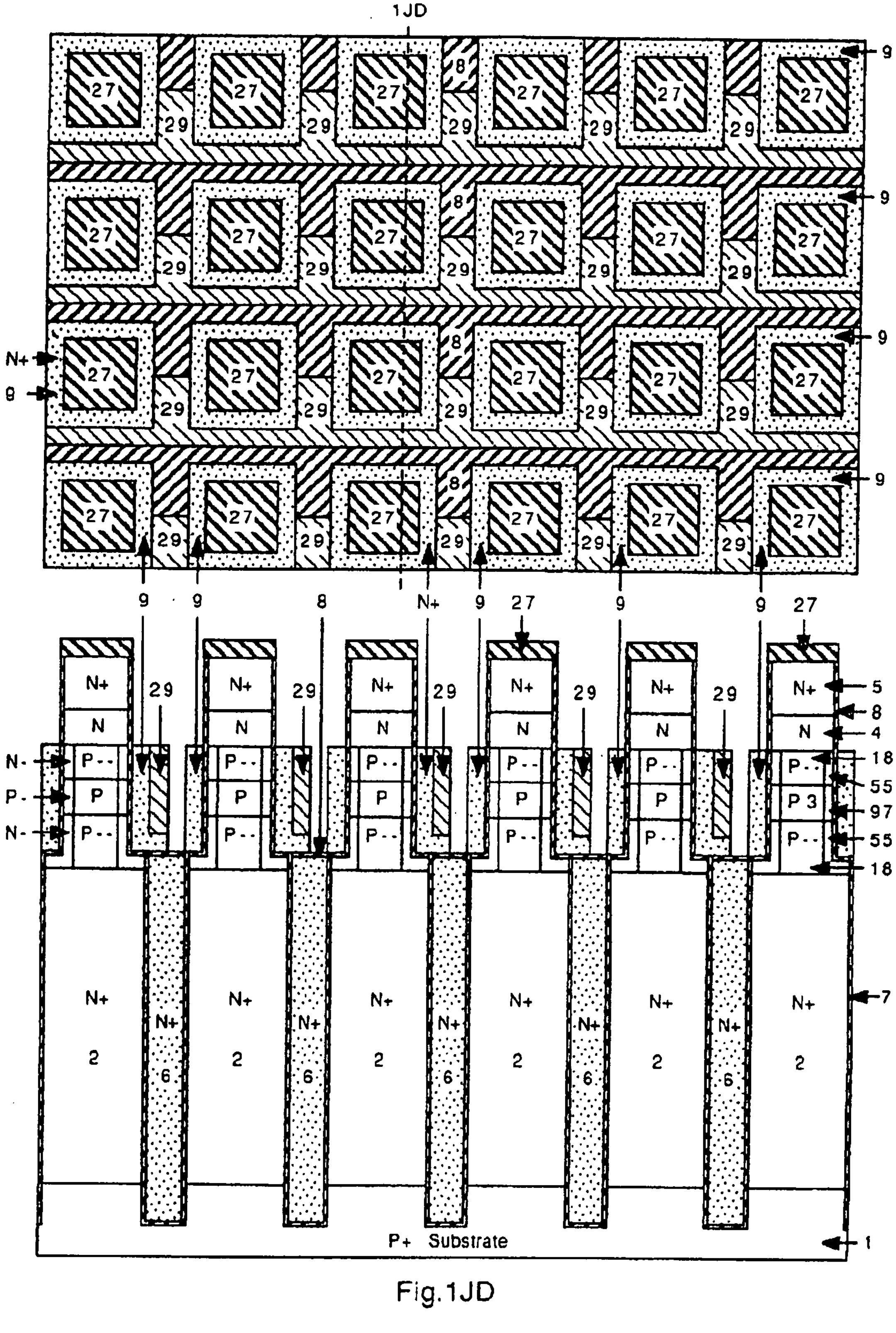

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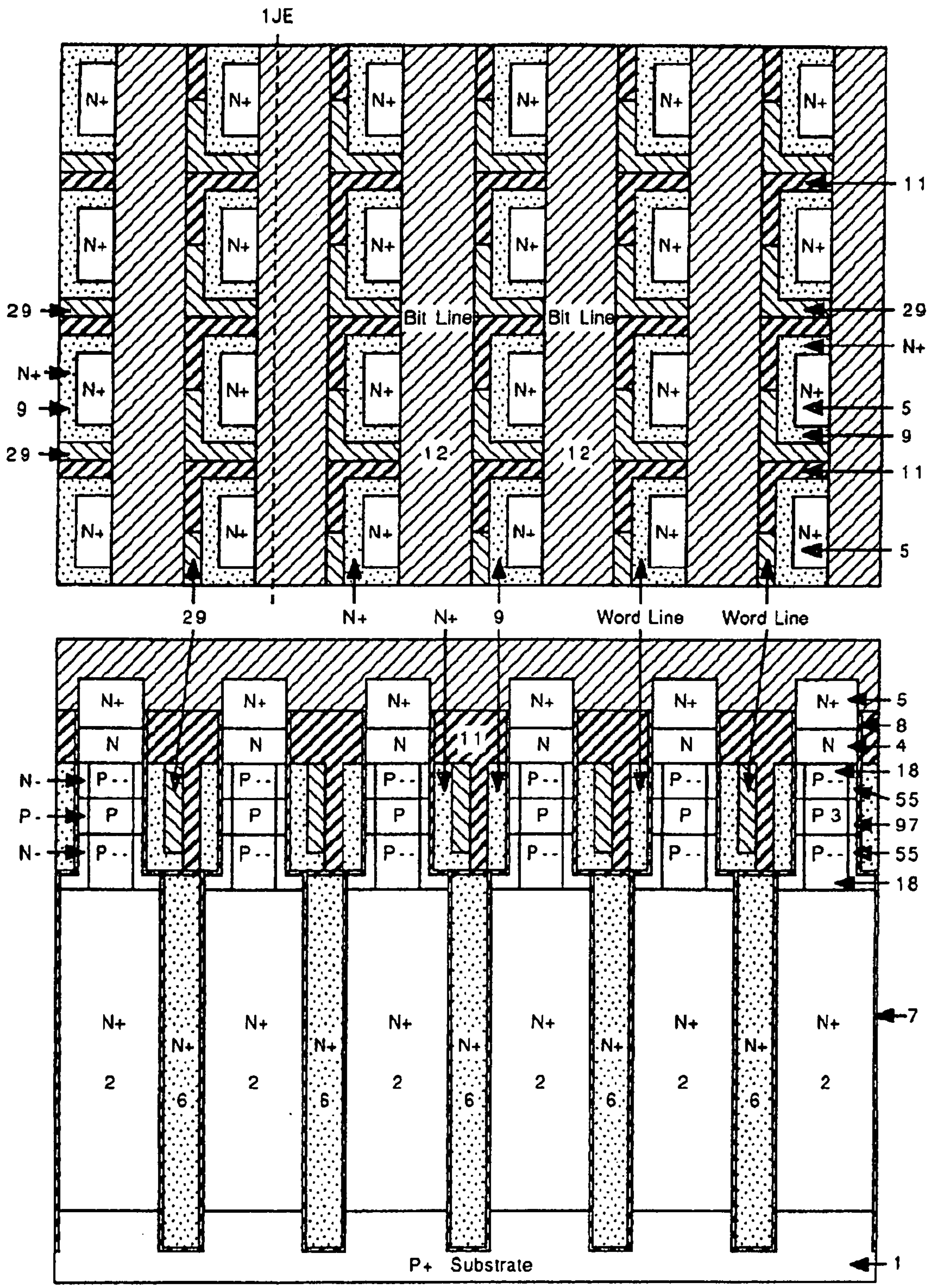
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Fig.1JE

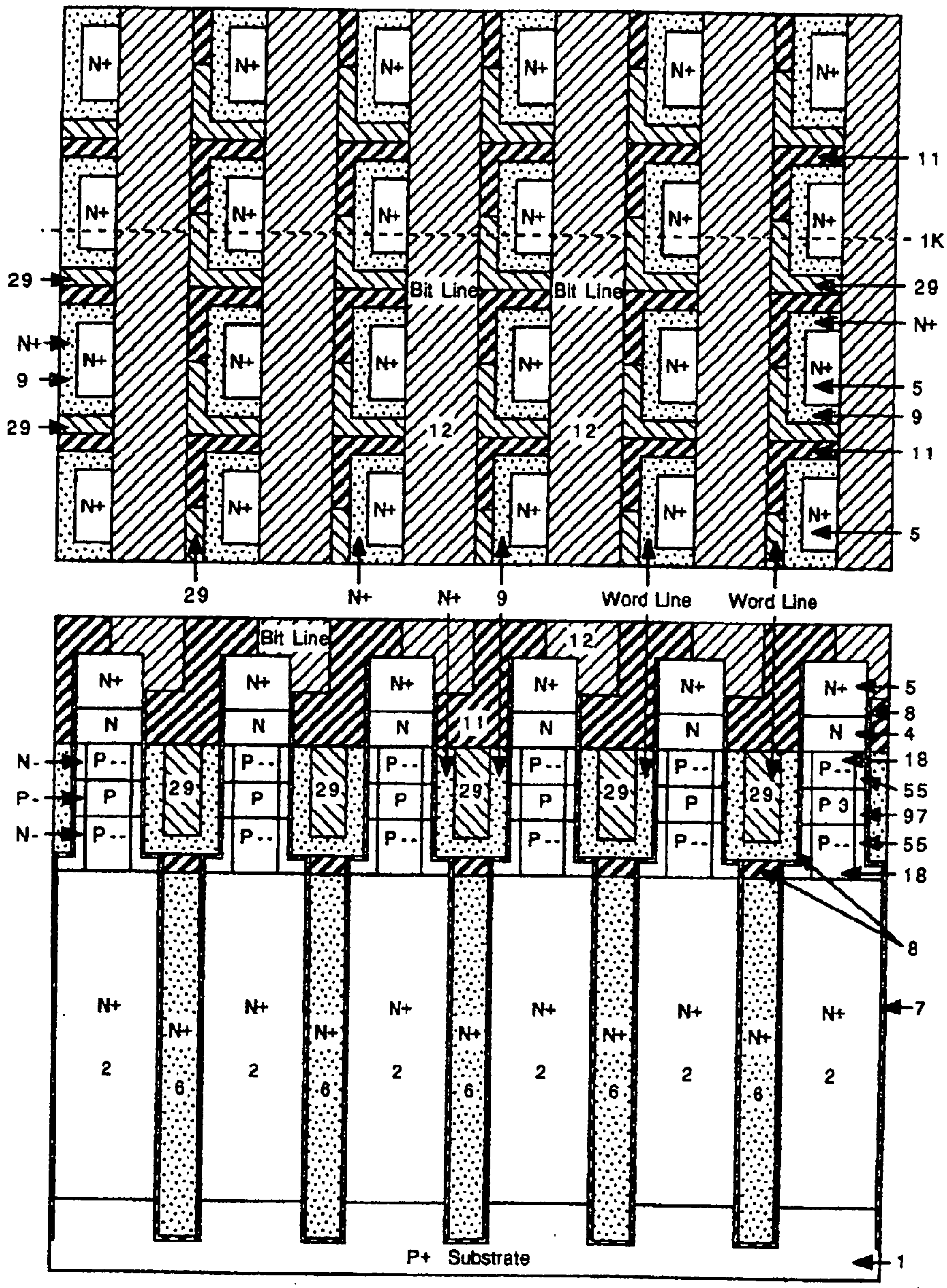
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Fig.1K

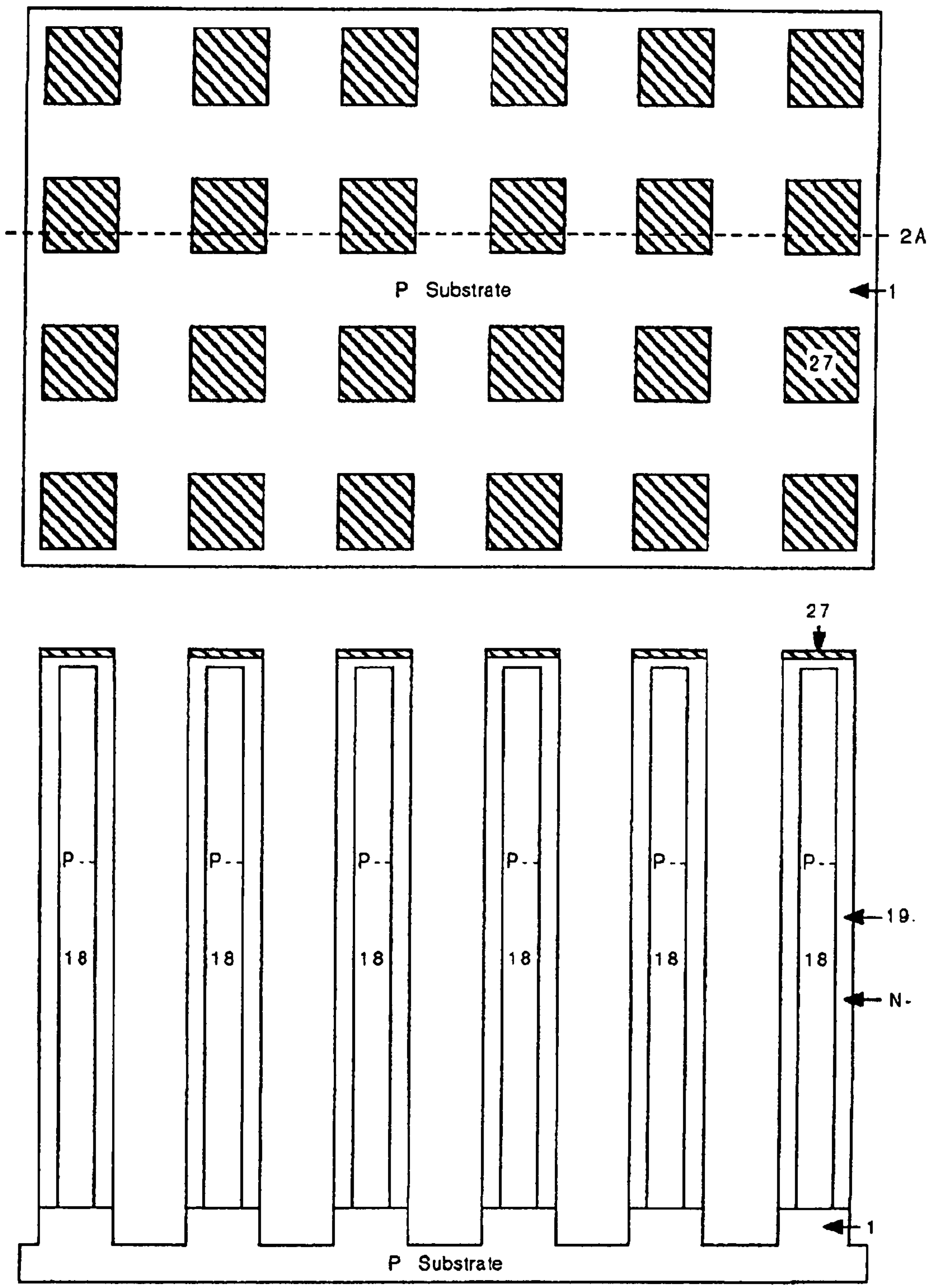


Fig.2A

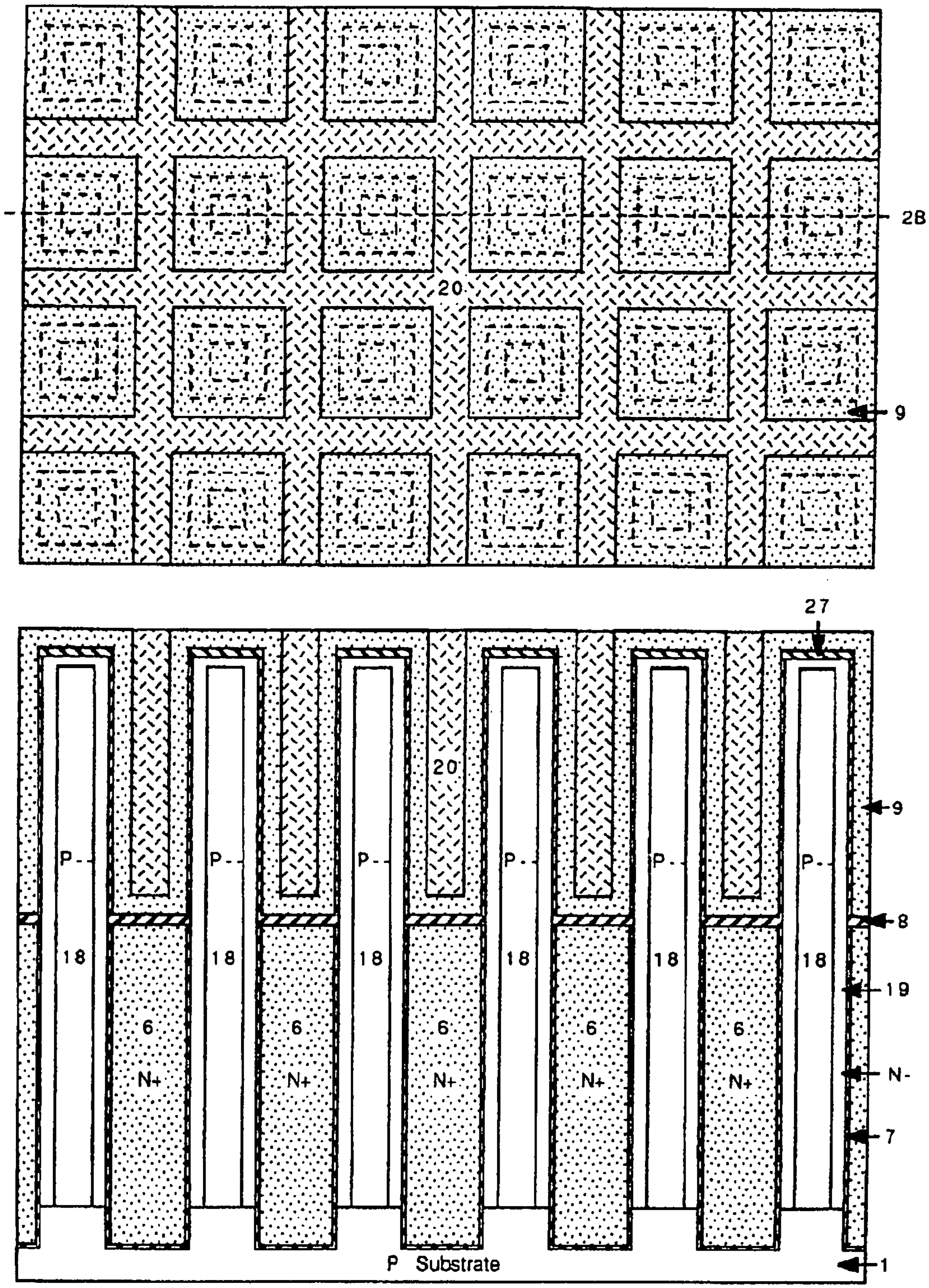


Fig.2B

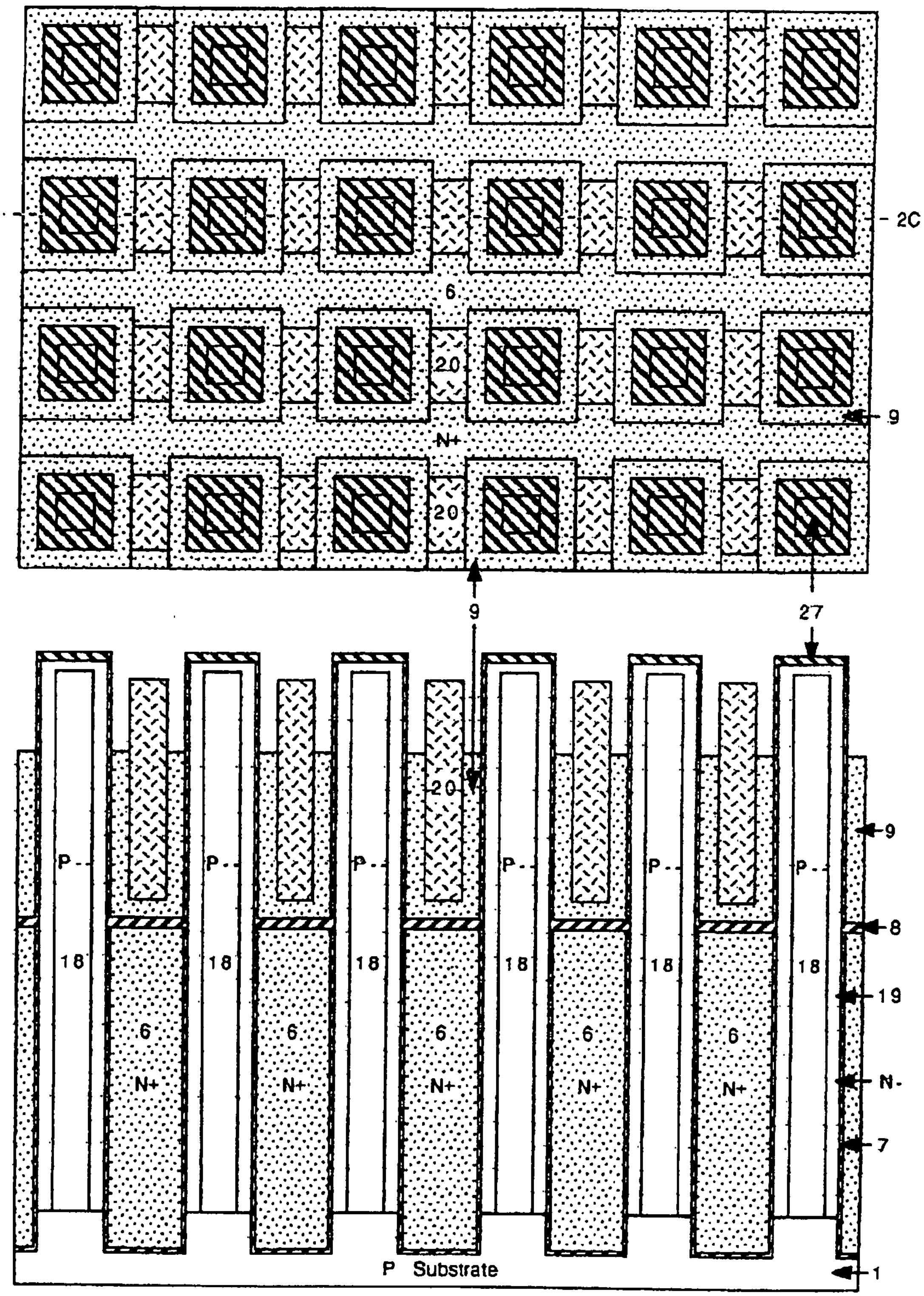
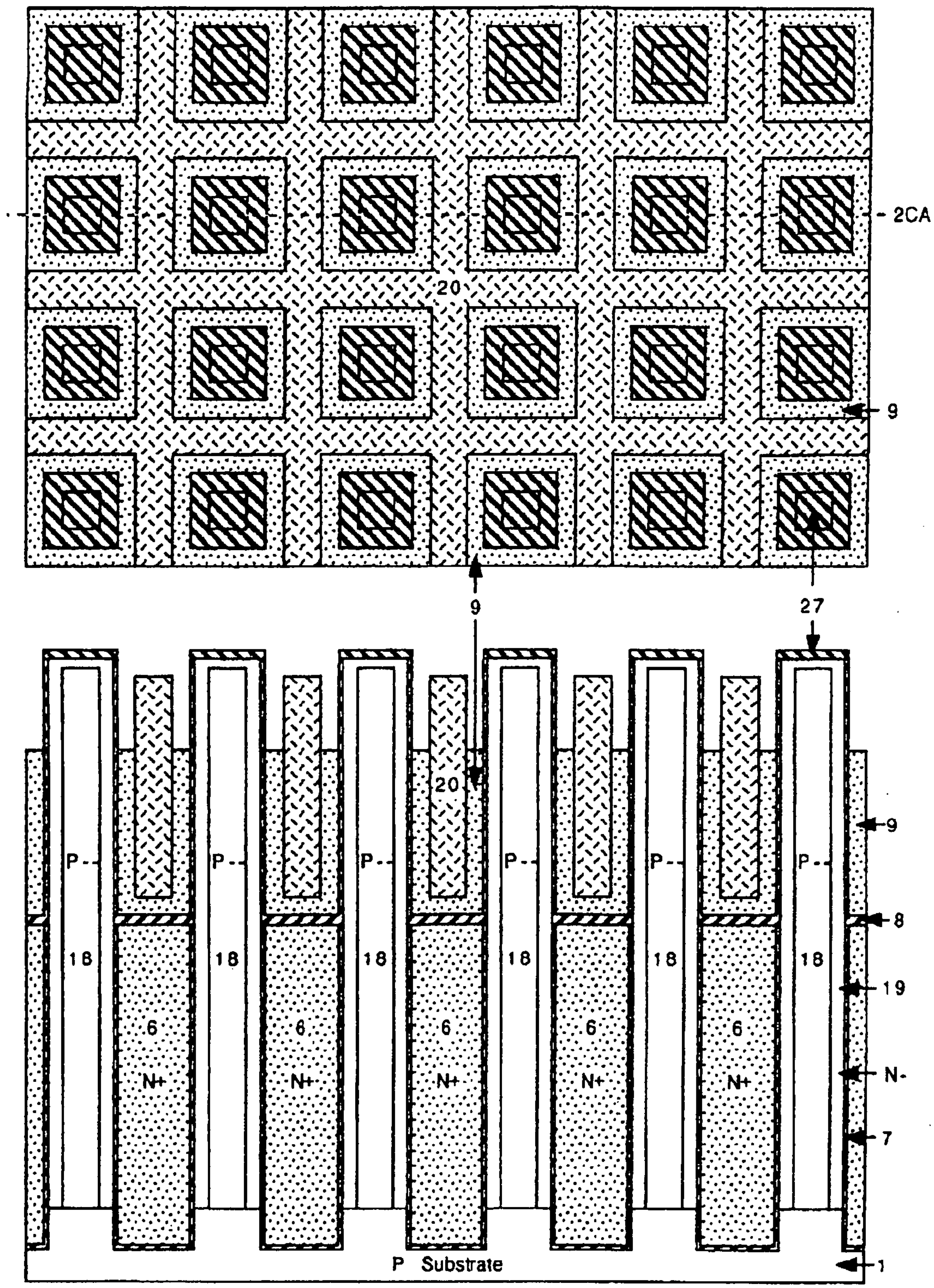


Fig.2C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P Substrate
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Fig.2CA

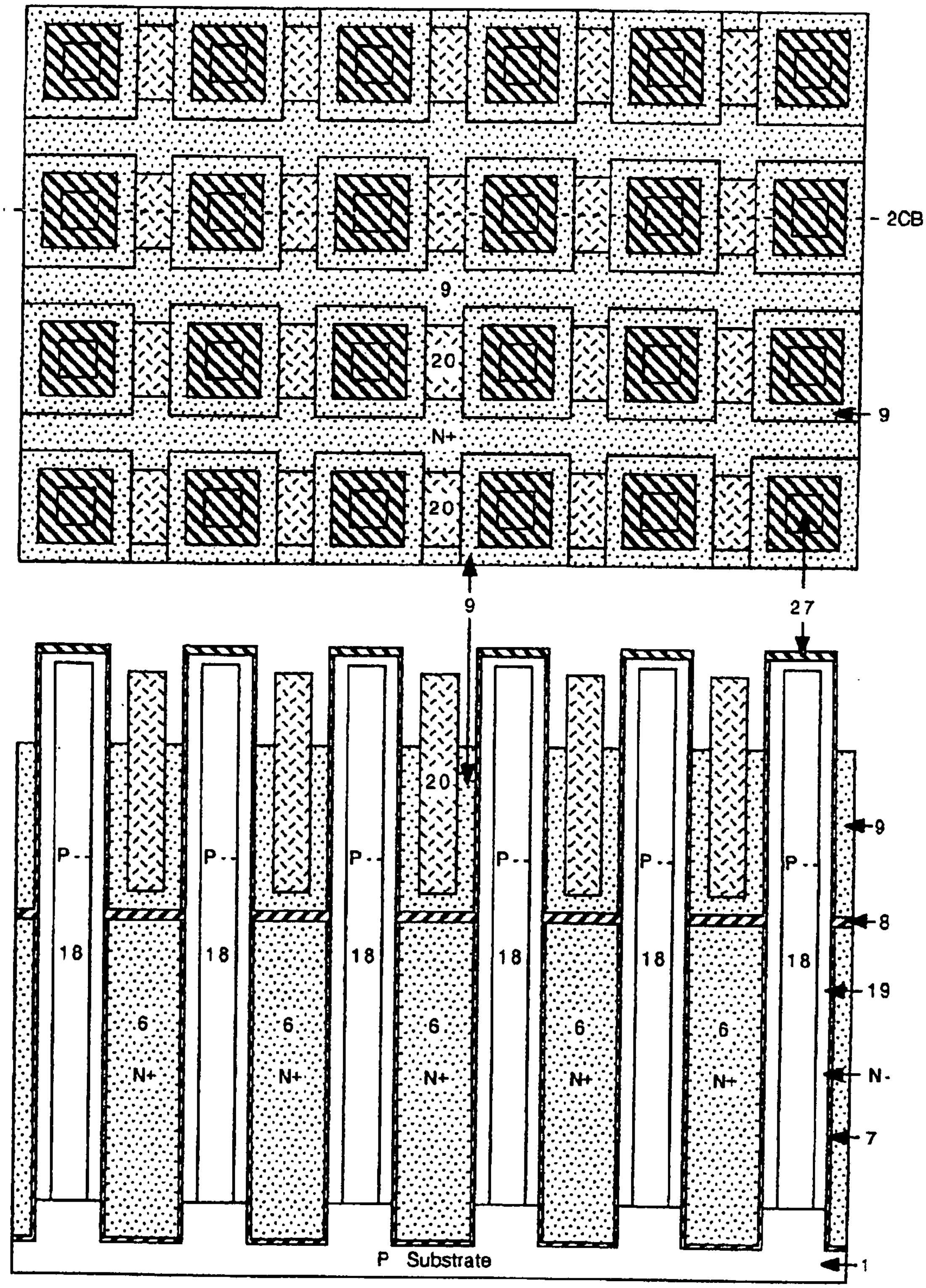


Fig.2CB

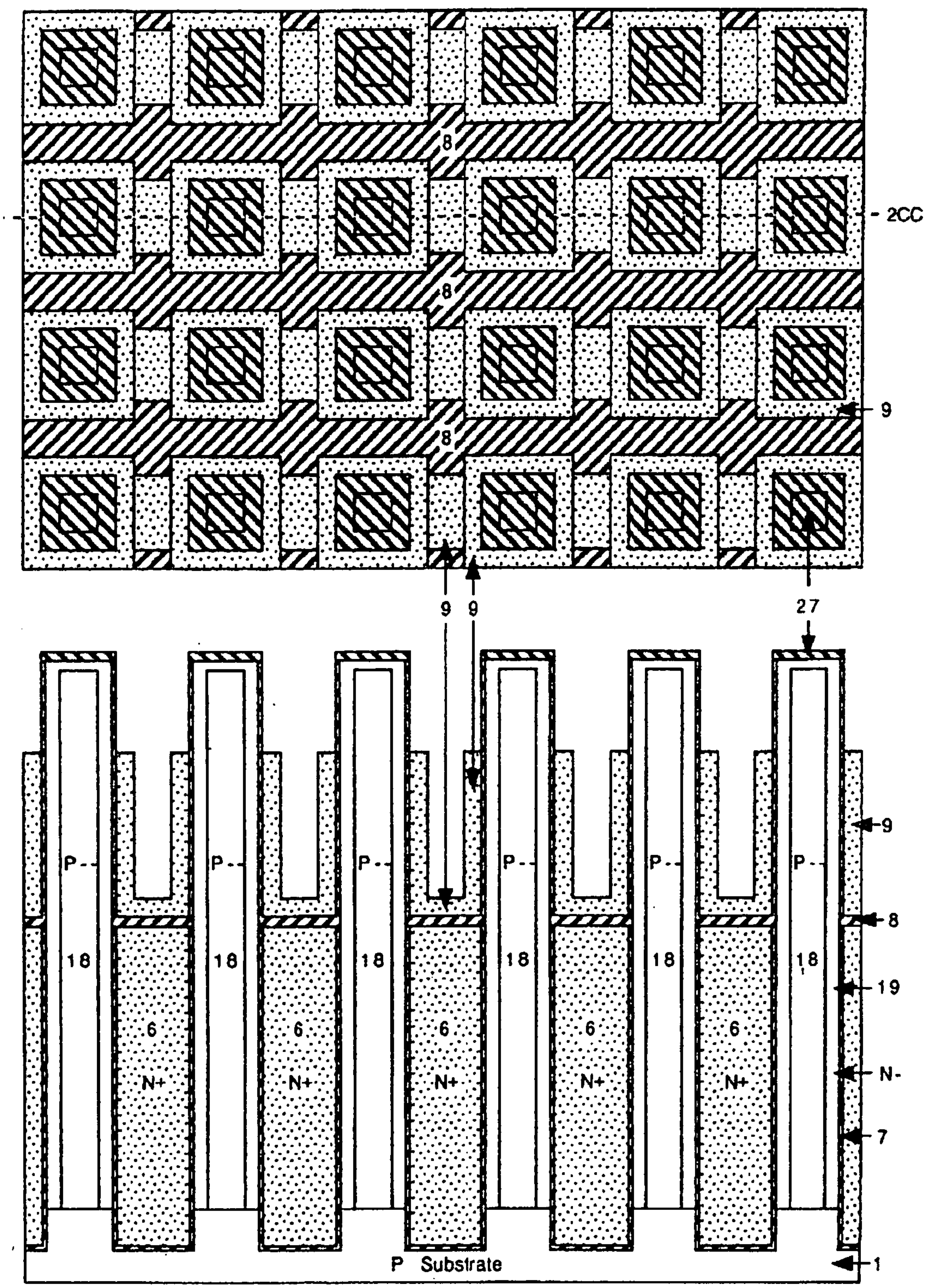
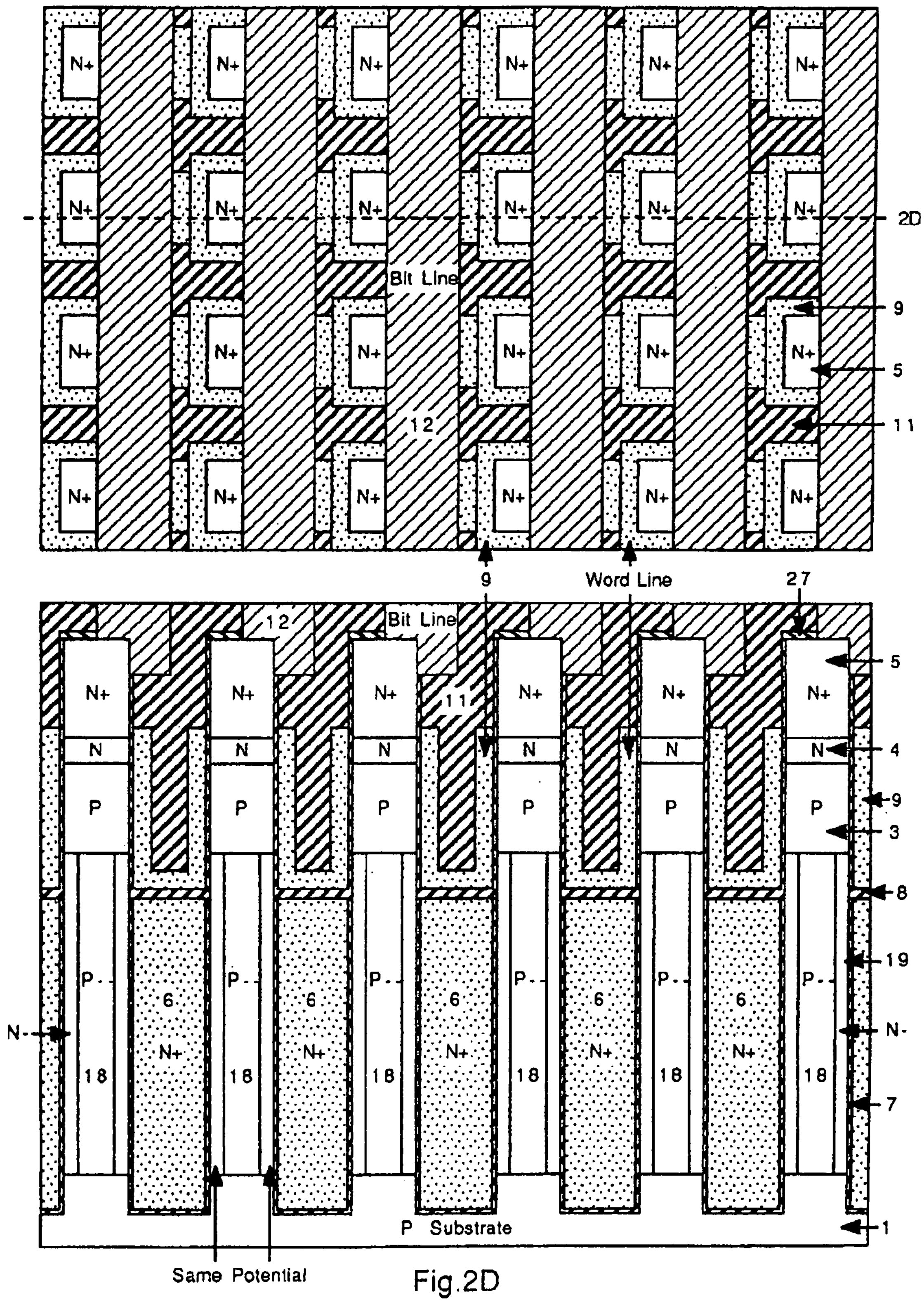


Fig.2CC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8
19
P-
6
N+
18
N-
7
P Substrate
1
Same Potential

Fig.2D

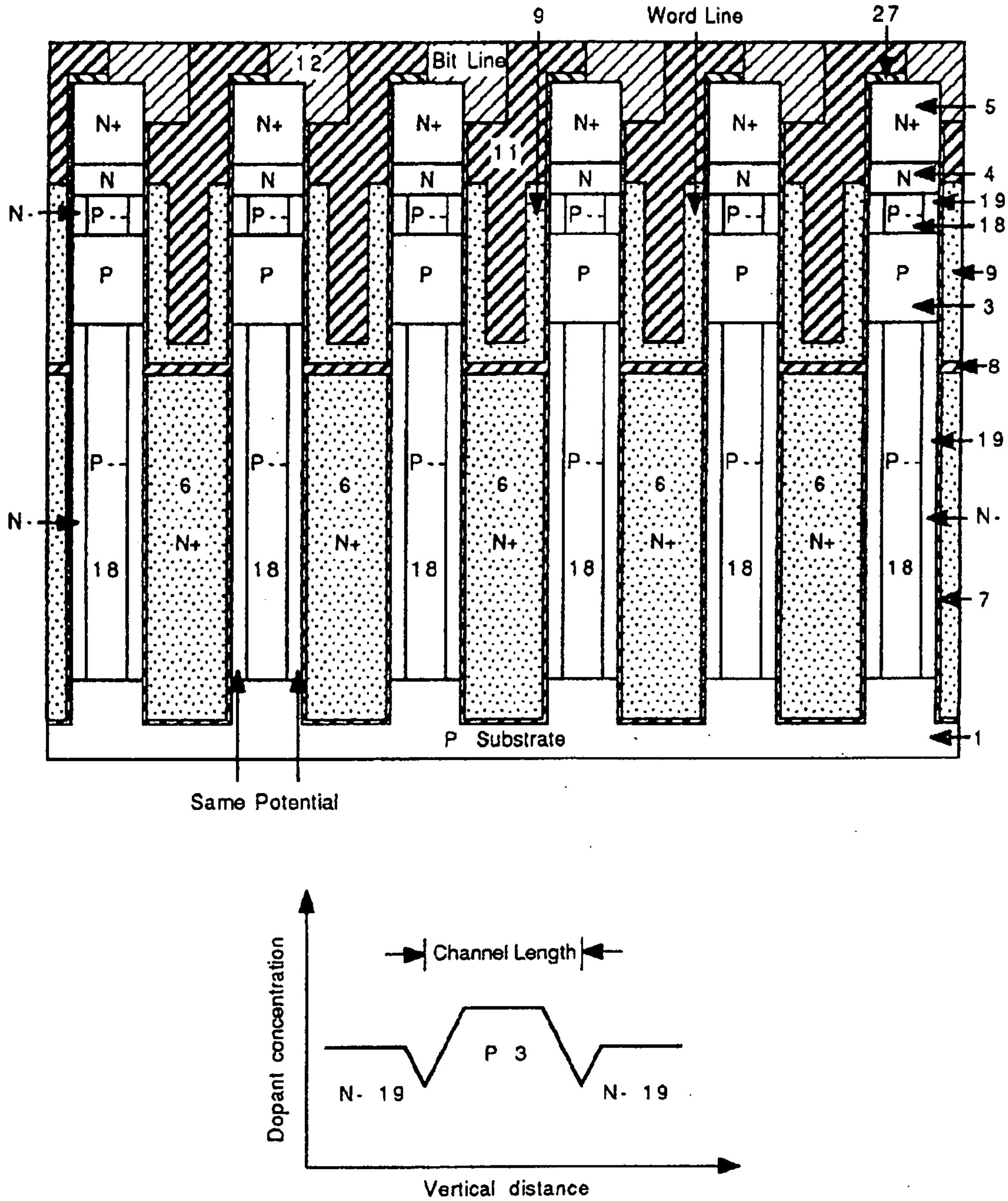

9
Word Line
27
12
Bit Line
11
N+
N
P--
P
N-
6
N+
18
5
4
19
18
9
3
8
19
N-
7
1
P Substrate
Same Potential
Channel Length
Dopant concentration
P 3
N- 19
N- 19
Vertical distance

Fig.3

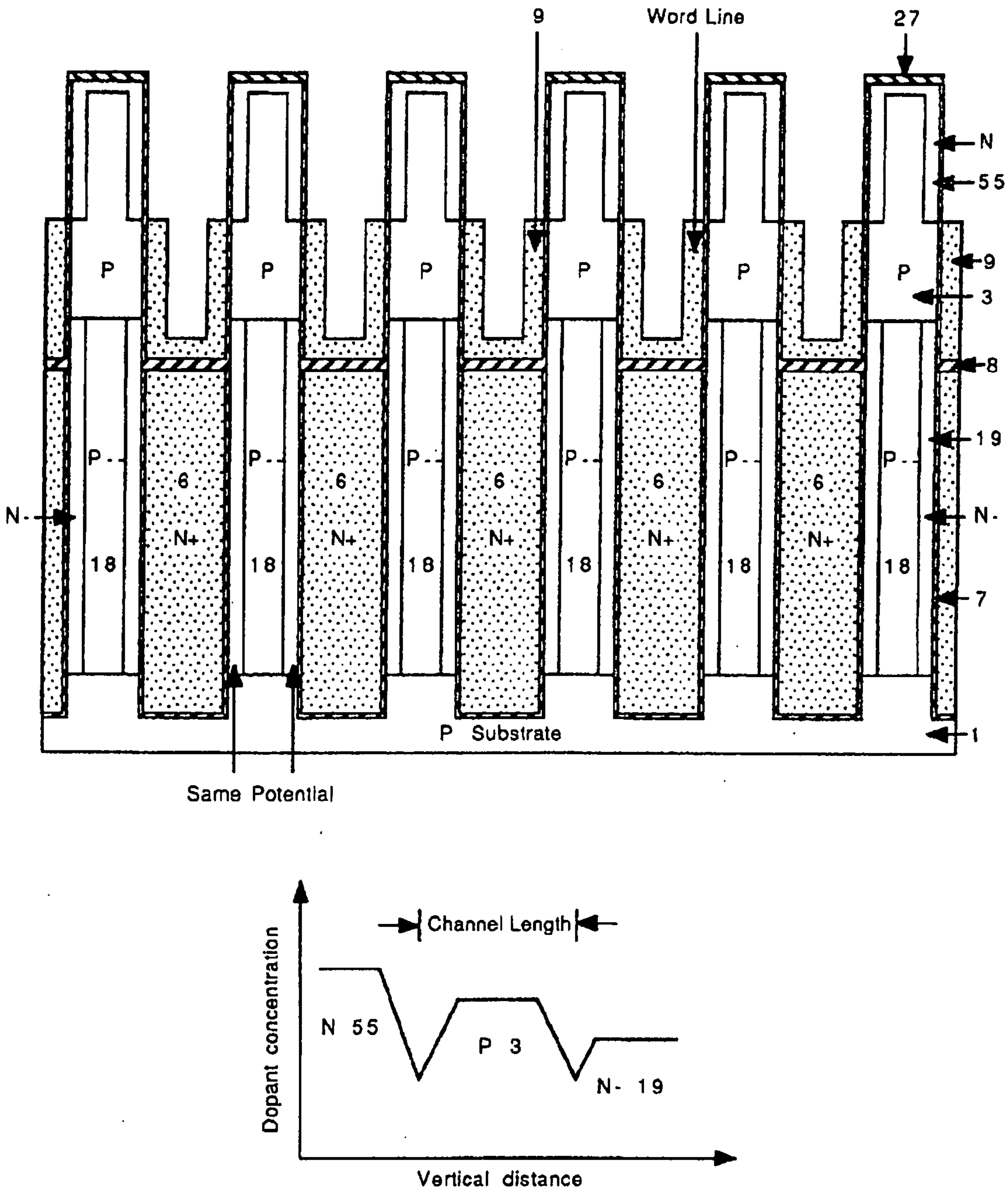

9
Word Line
27
N
55
P
9
3
8
19
P--
6
N+
18
N-
7
P Substrate
1
Same Potential
Channel Length
Dopant concentration
N 55
P 3
N- 19
Vertical distance

Fig.4A

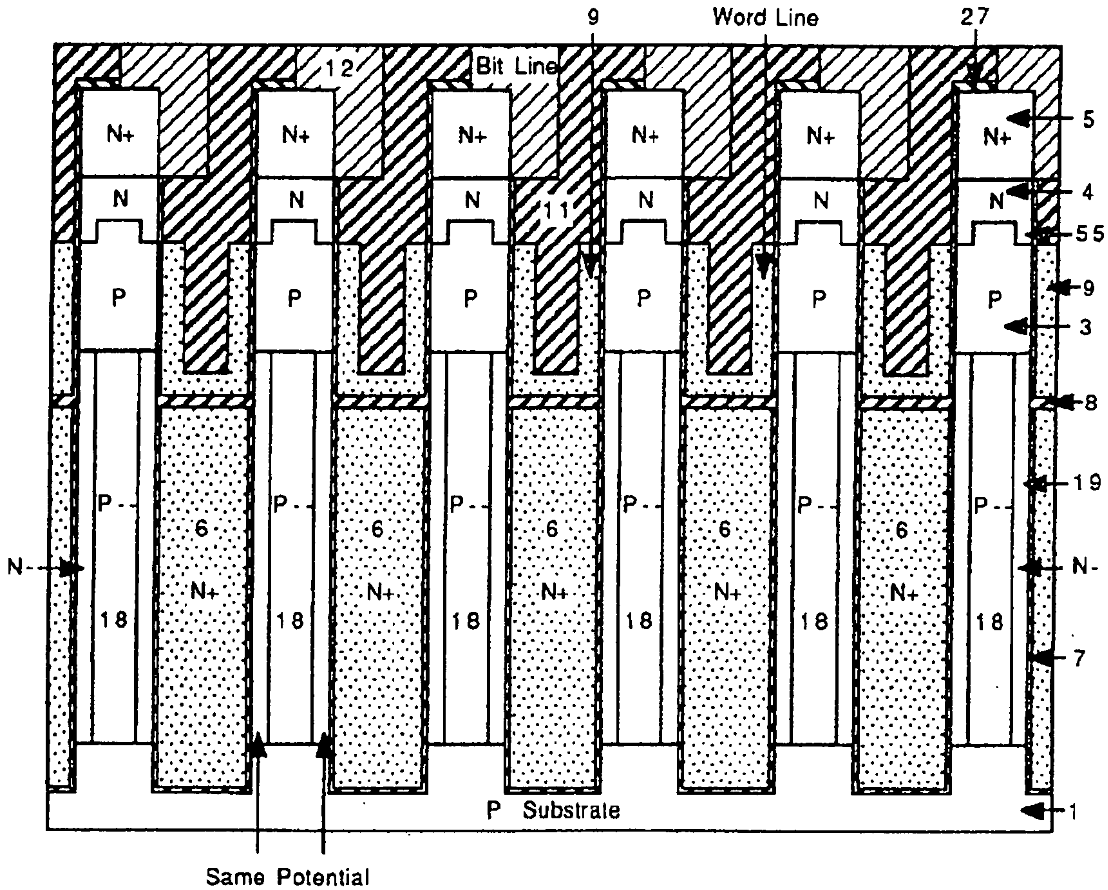

9
Word Line
27
12
Bit Line
N+
N
P
11
5
4
55
9
3
8
19
P--
6
N+
18
N-
7
P Substrate
1
Same Potential

Fig.4B

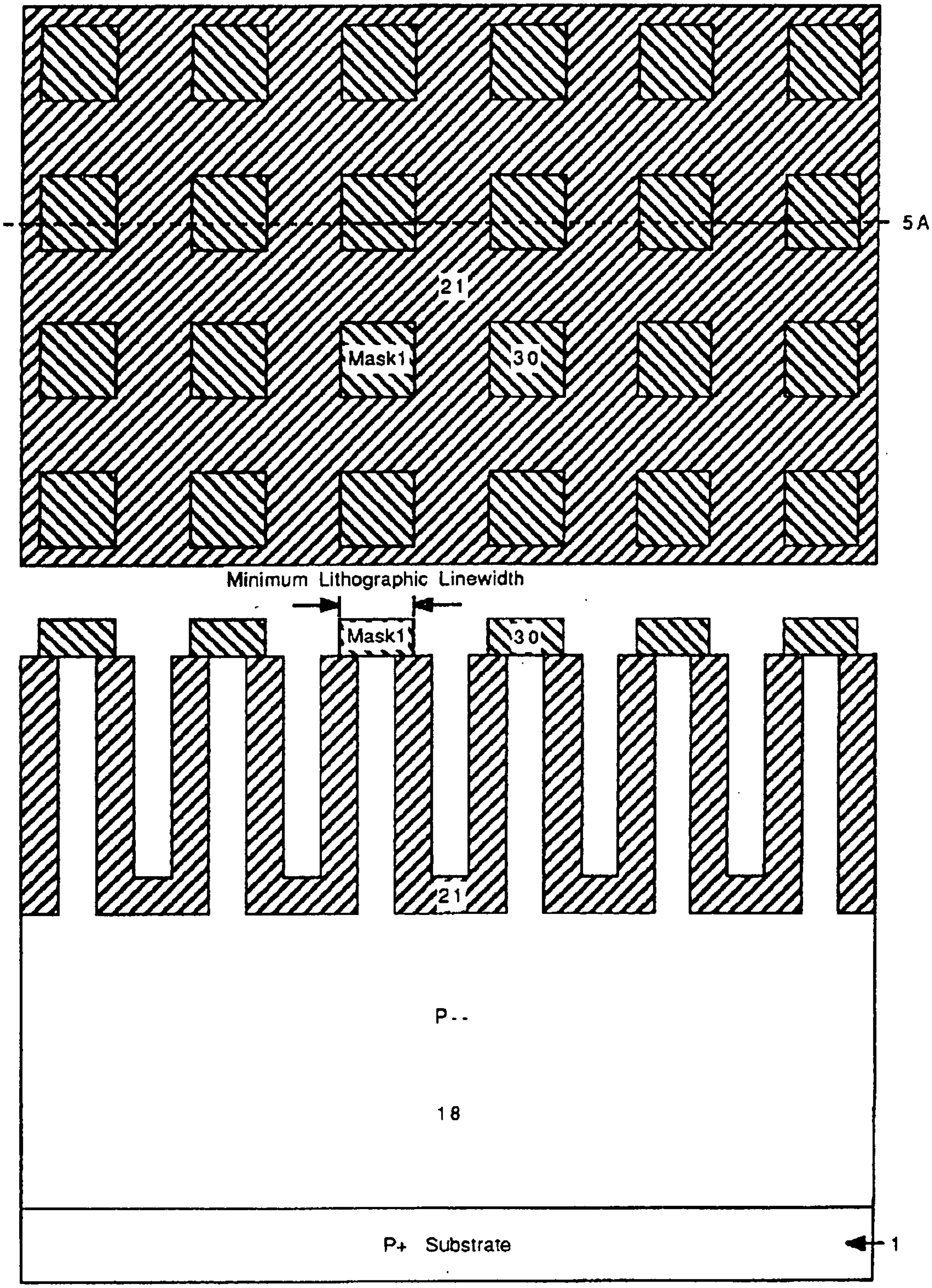

5A
21
Mask1
30
Minimum Lithographic Linewidth
Mask1
30
21
P--
18
P+ Substrate
1

Fig.5A

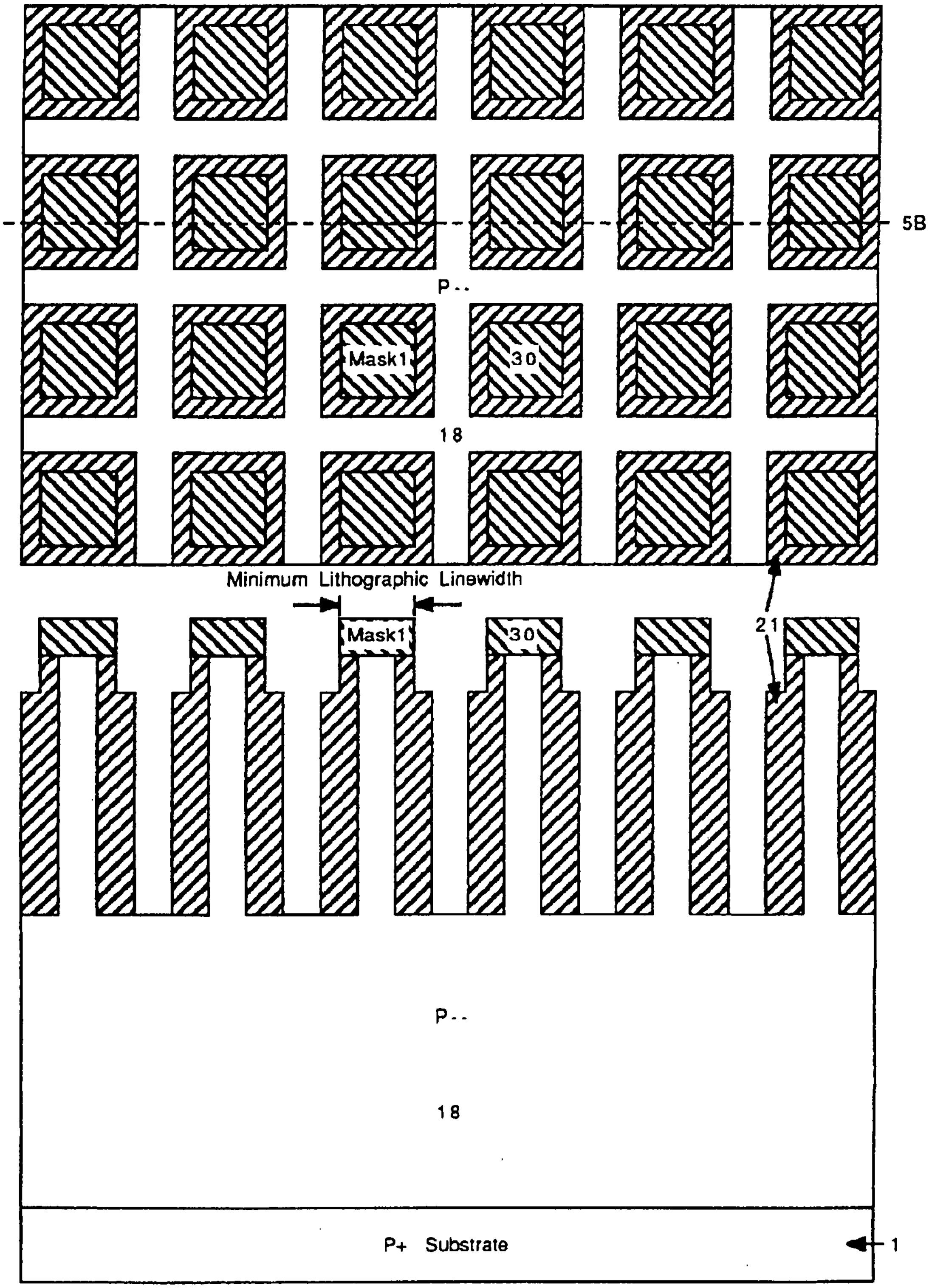

5B
P--
Mask1
30
18
Minimum Lithographic Linewidth
Mask1
30
21
P--
18
P+ Substrate
1

Fig.5B

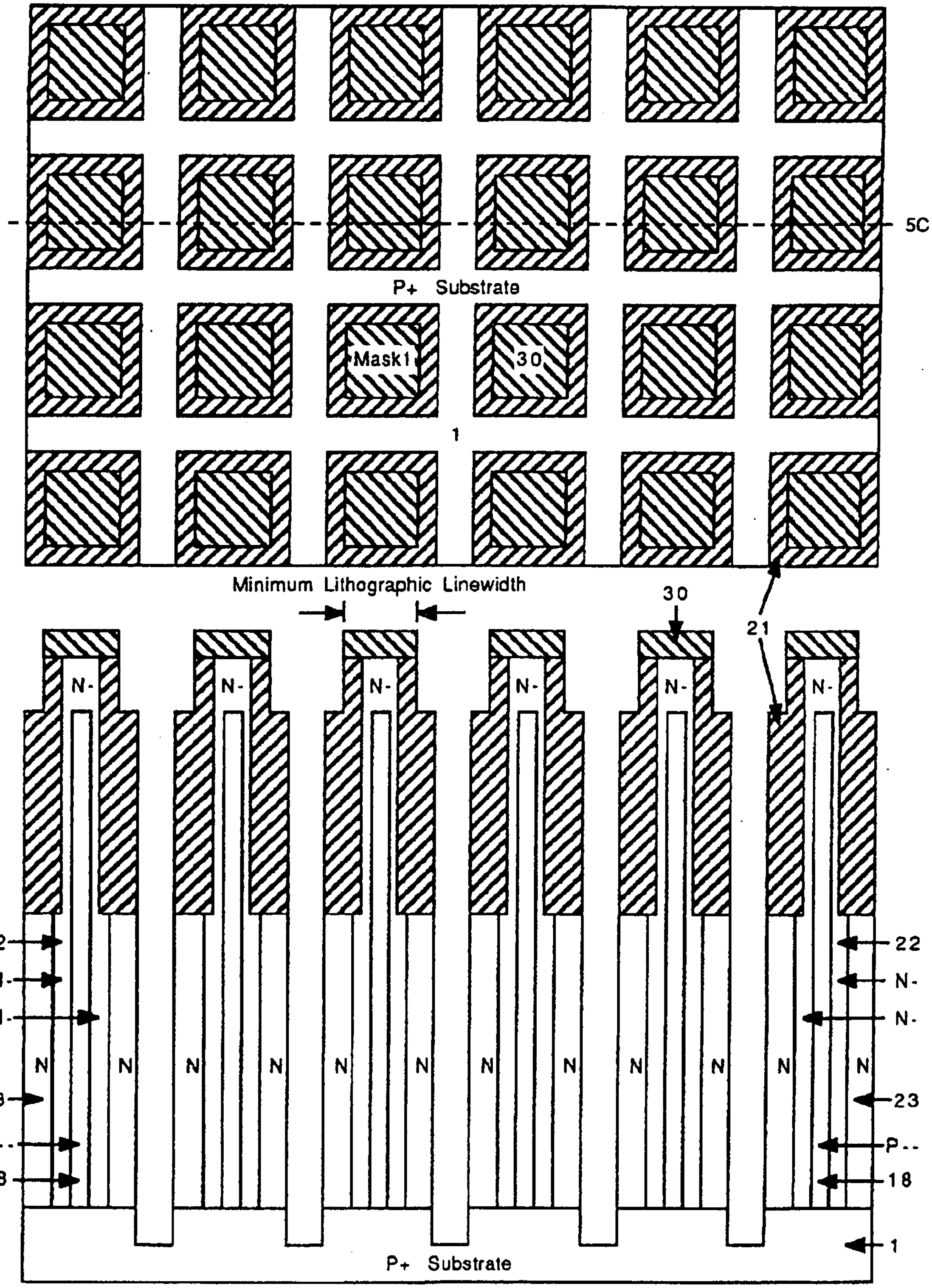

5C
P+ Substrate
Mask1
30
1
Minimum Lithographic Linewidth
30
21
N-
22
N-
N-
N
23
P--
18
22
N-
N-
N
23
P--
18
1
P+ Substrate

Fig.5C

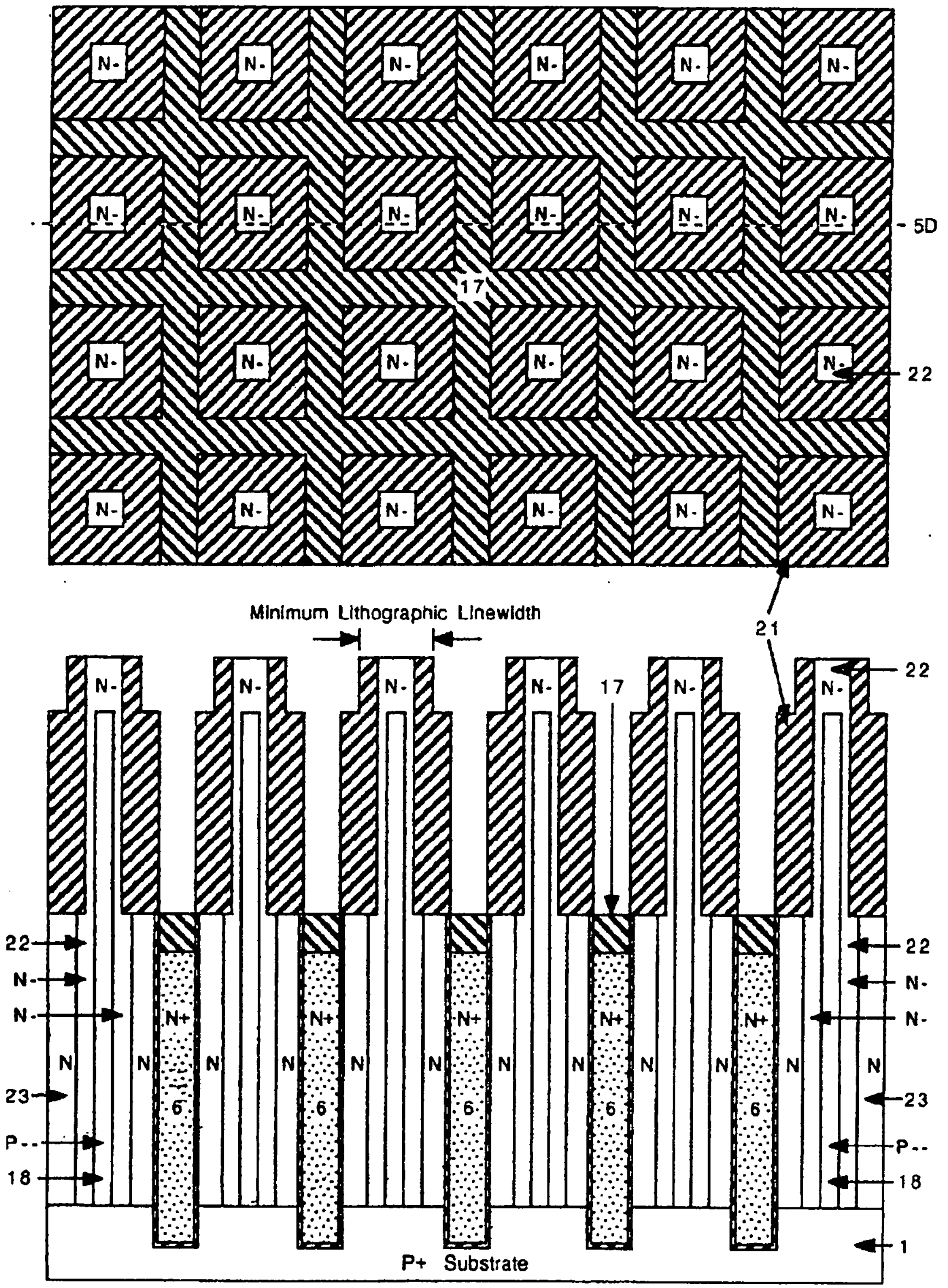

N-
5D
17
22
Minimum Lithographic Linewidth
21
N-
17
22
N+
N
6
23
P--
18
1
P+ Substrate

Fig.5D

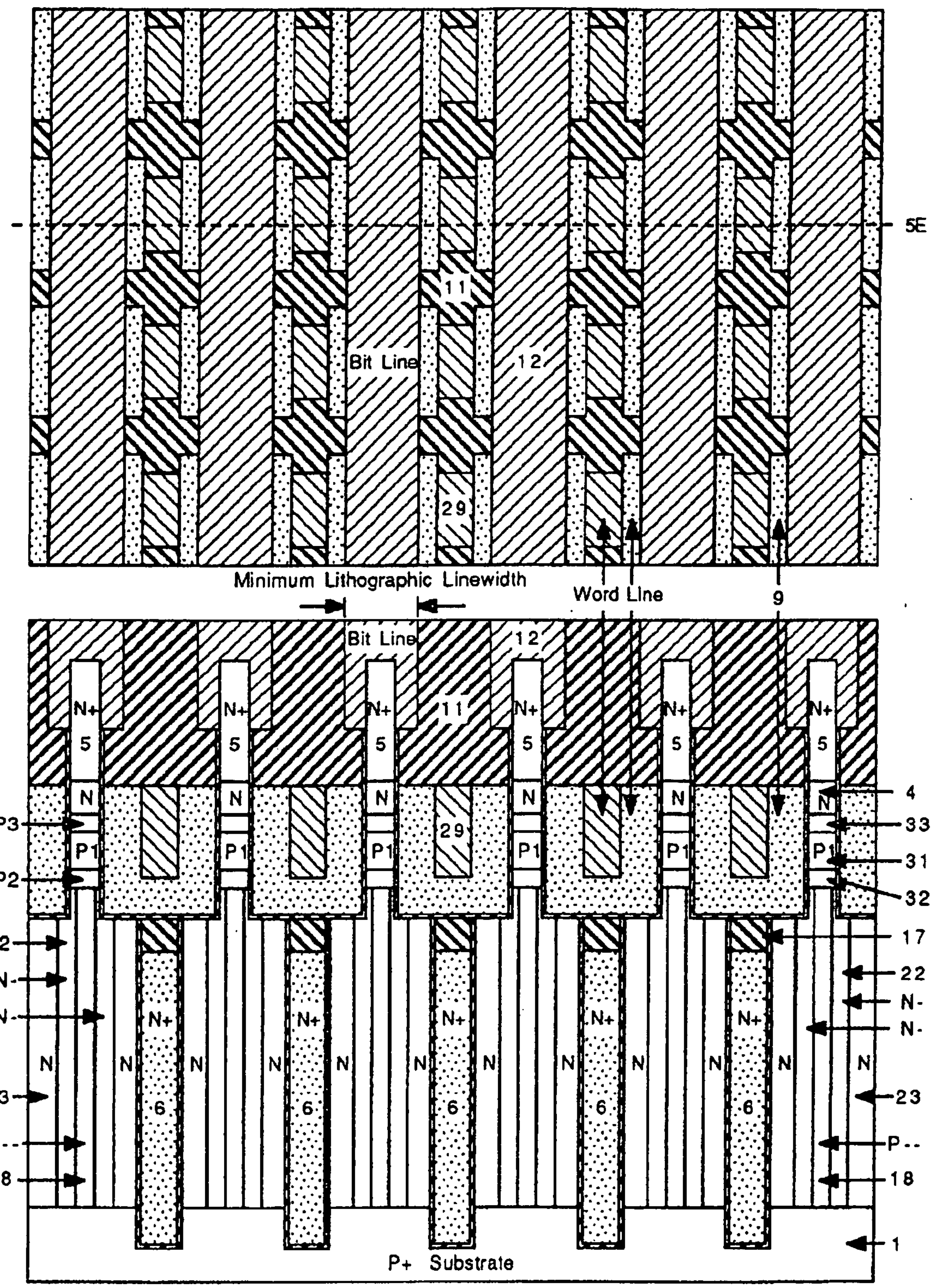

5E
11
Bit Line
12
29
Minimum Lithographic Linewidth
Word Line
9
Bit Line
12
N+
5
11
N
P3
P1
P2
29
4
33
31
32
22
N-
N-
N+
N
17
22
N-
N-
6
23
23
P--
P--
18
18
1
P+ Substrate

Fig.5E

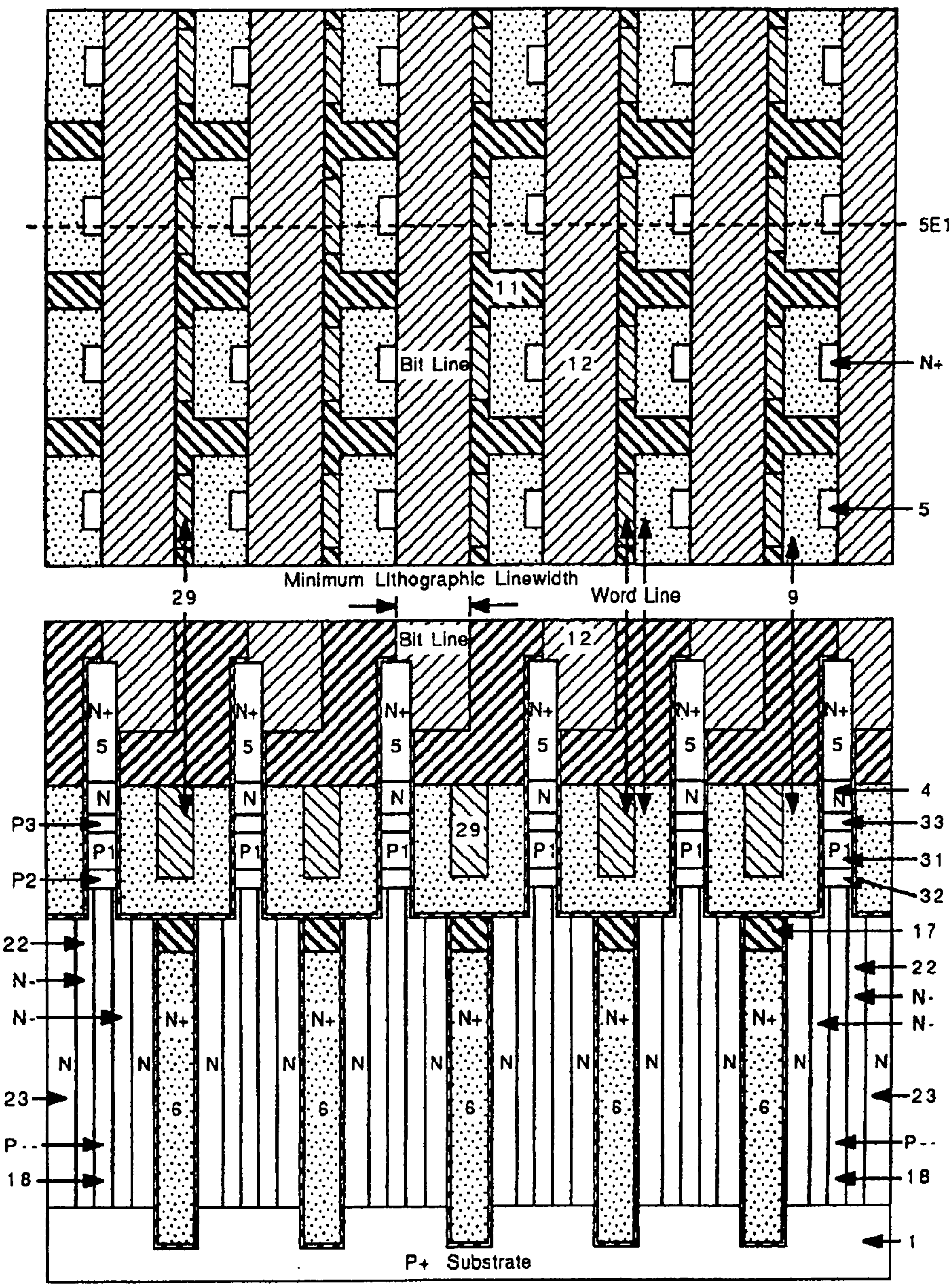
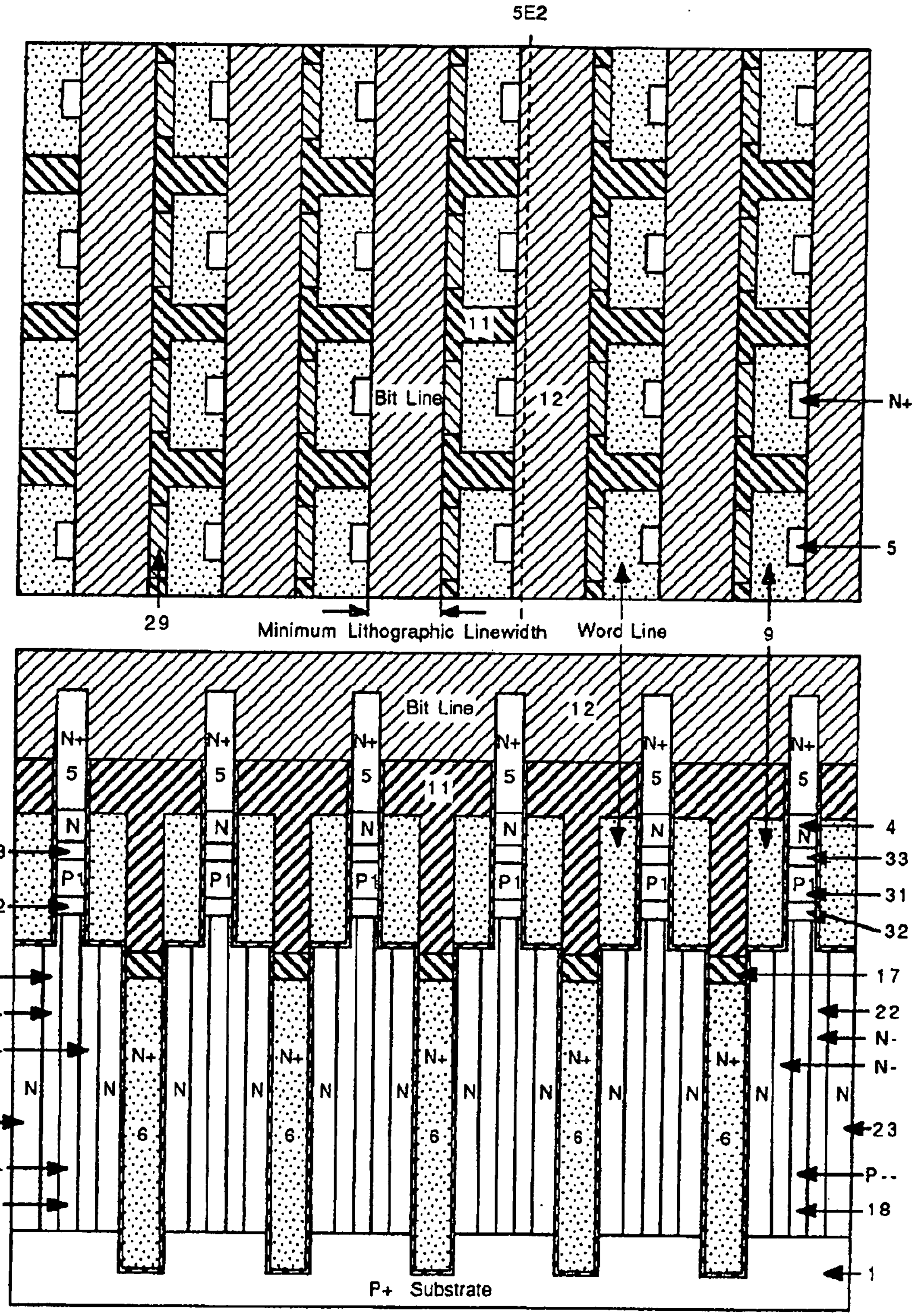

5E1
11
Bit Line
12
N+
5
29
Minimum Lithographic Linewidth
Word Line
9
Bit Line
12
N+
5
N
P3
P1
P2
29
4
33
31
32
17
22
N-
N-
N
N+
6
23
P--
18
1
P+ Substrate

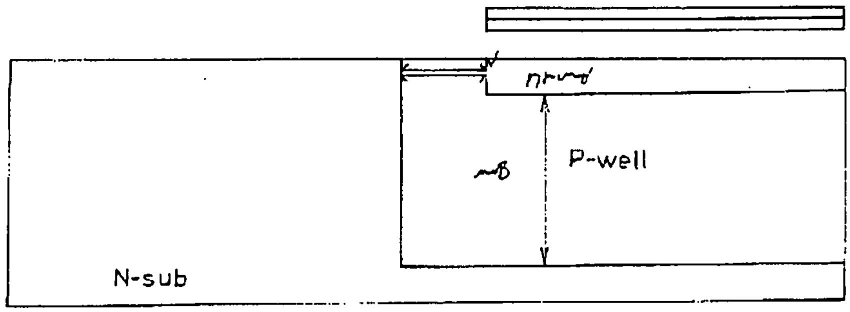
Fig.5E1



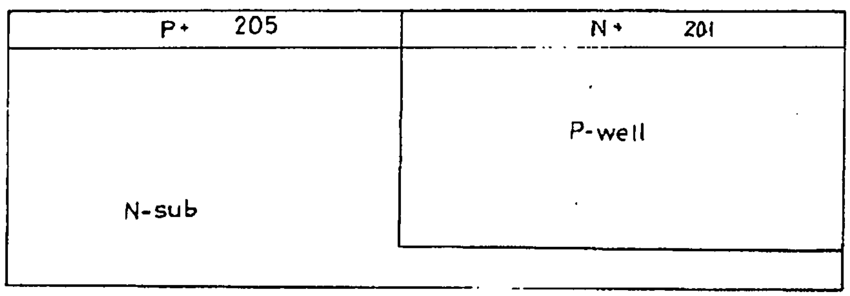
5E2
11
Bit Line
12
N+
5
29
Minimum Lithographic Linewidth
Word Line
9
Bit Line
12
N+
5
11
N
P1
P3
P2
4
33
31
32
17
22
N-
N
N+
6
23
P--
18
1
P+ Substrate

Fig.5E2

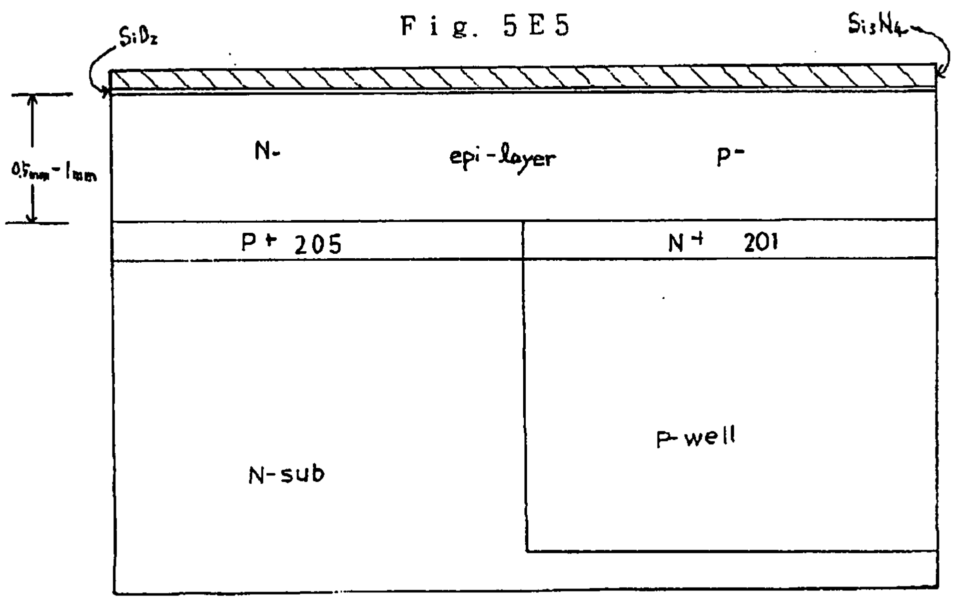
Ｆｉｇ．５Ｅ３



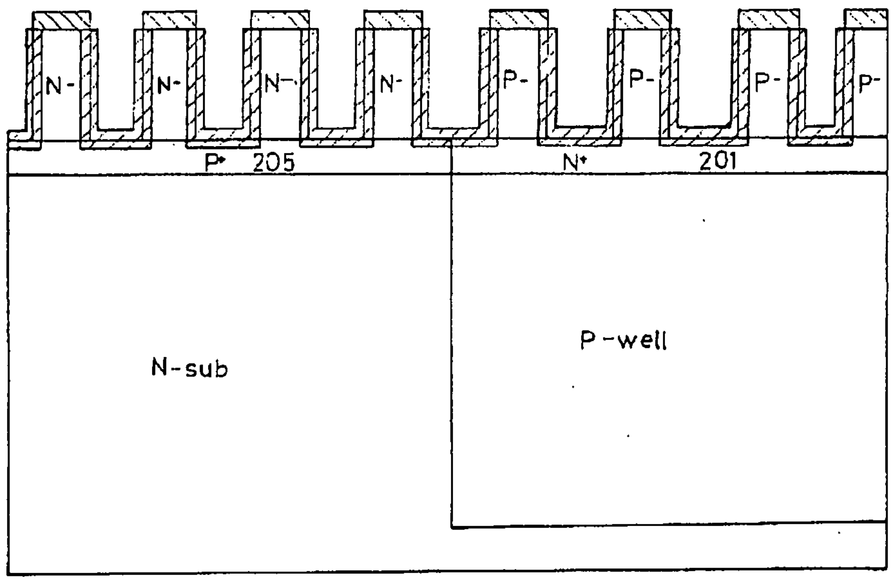
Ｆｉｇ．５Ｅ４



Ｆｉｇ．５Ｅ５



Ｆｉｇ．５Ｅ６



Ｆｉｇ．５Ｅ７

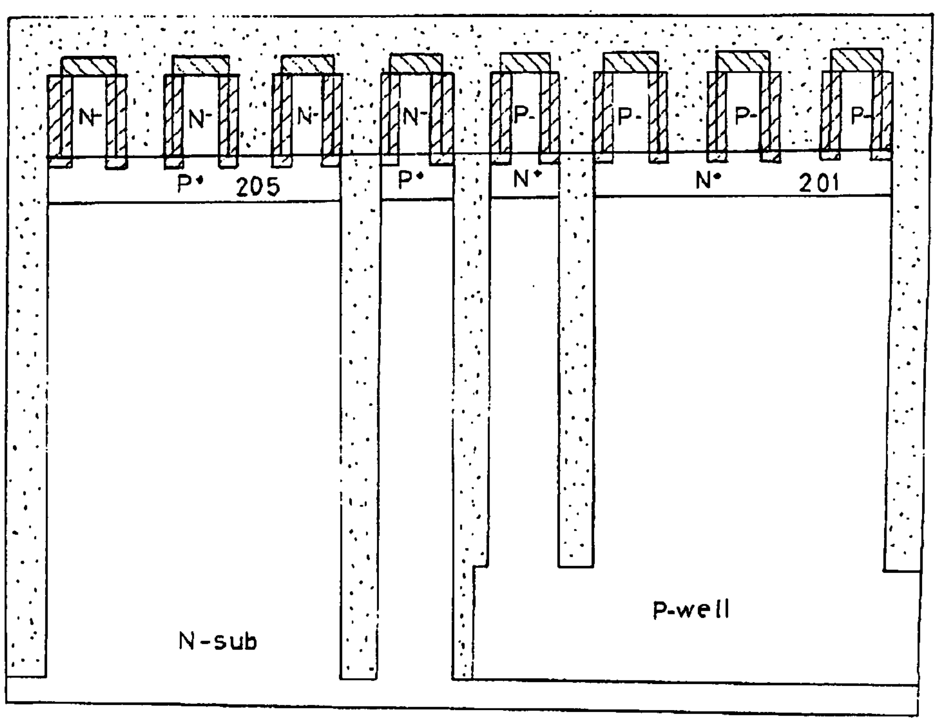


Fig. 5E8

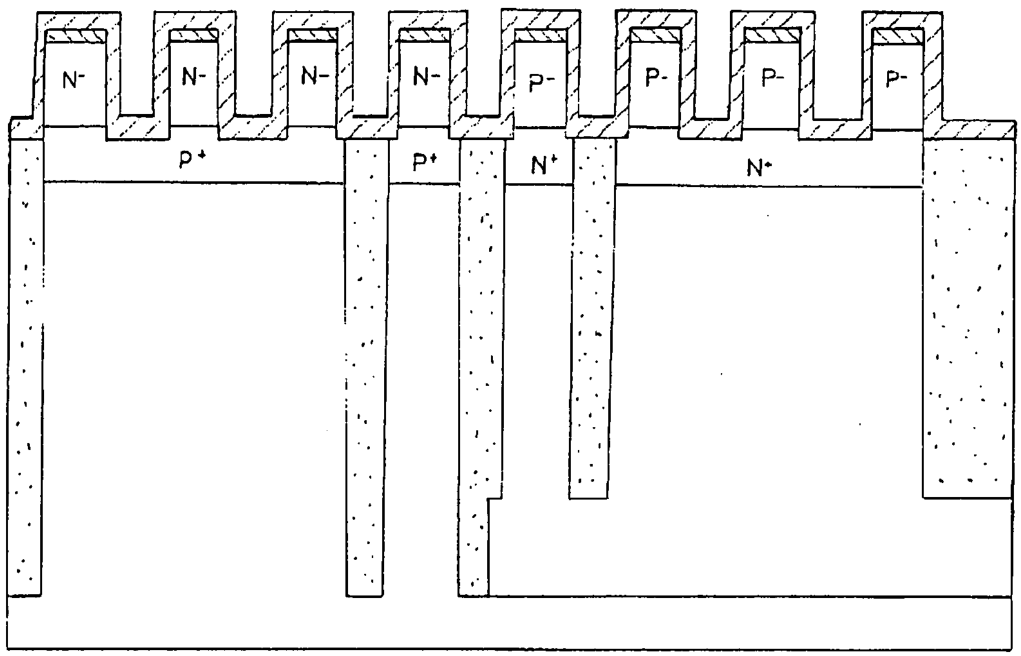
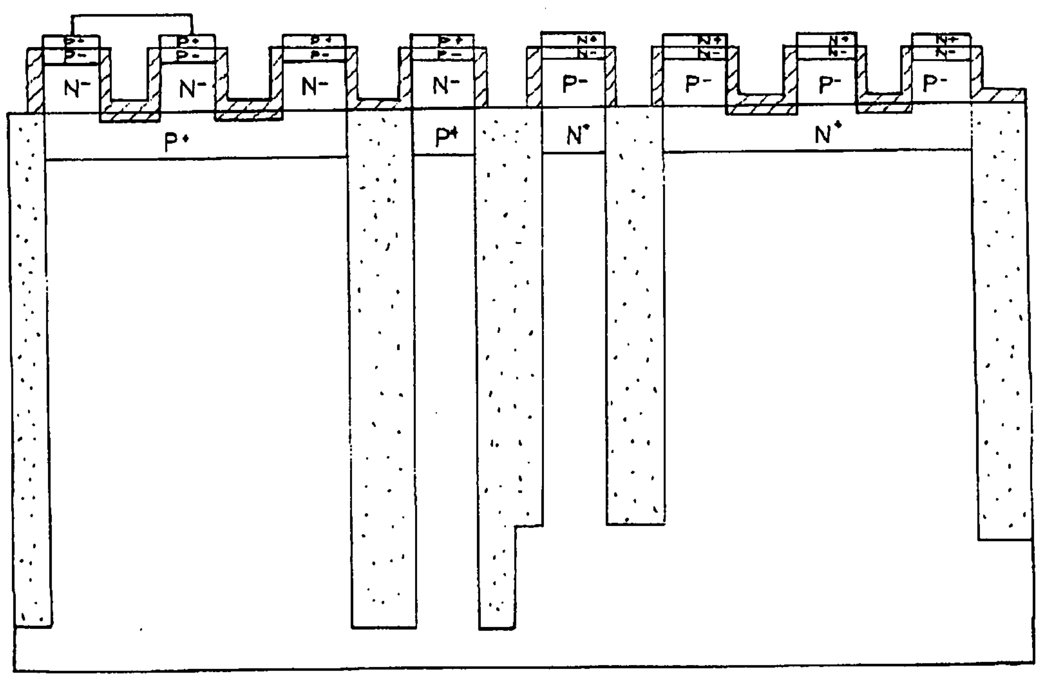


Fig. 5E9



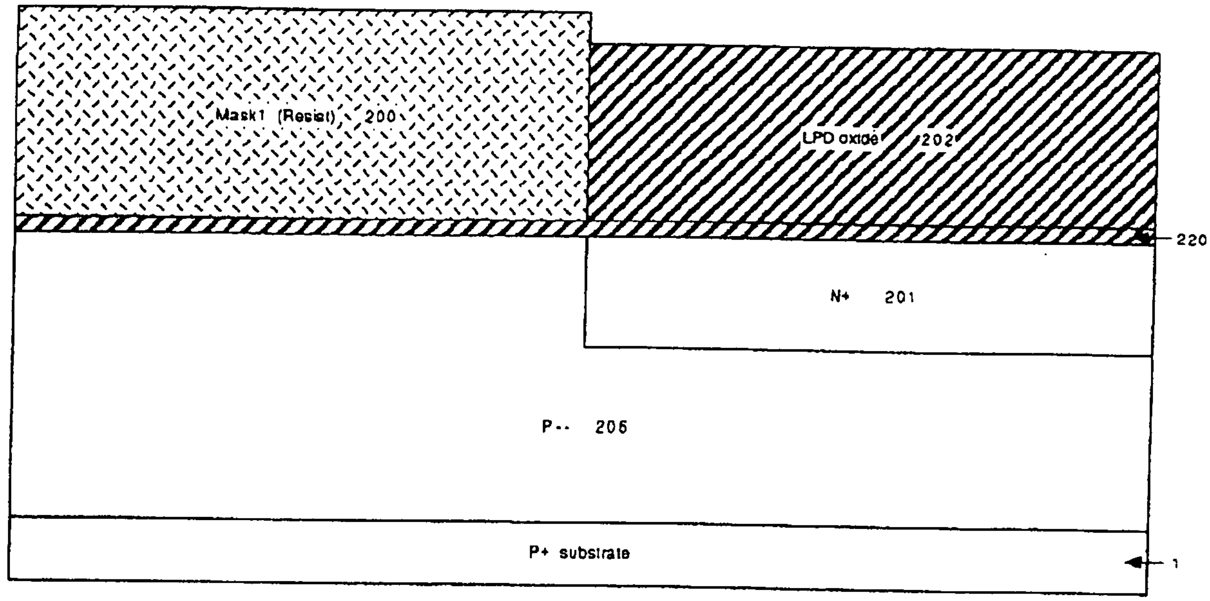

Mask1 (Resist) 200
LPD oxide 202
220
N+ 201
P-- 206
P+ substrate
1

Fig.6A

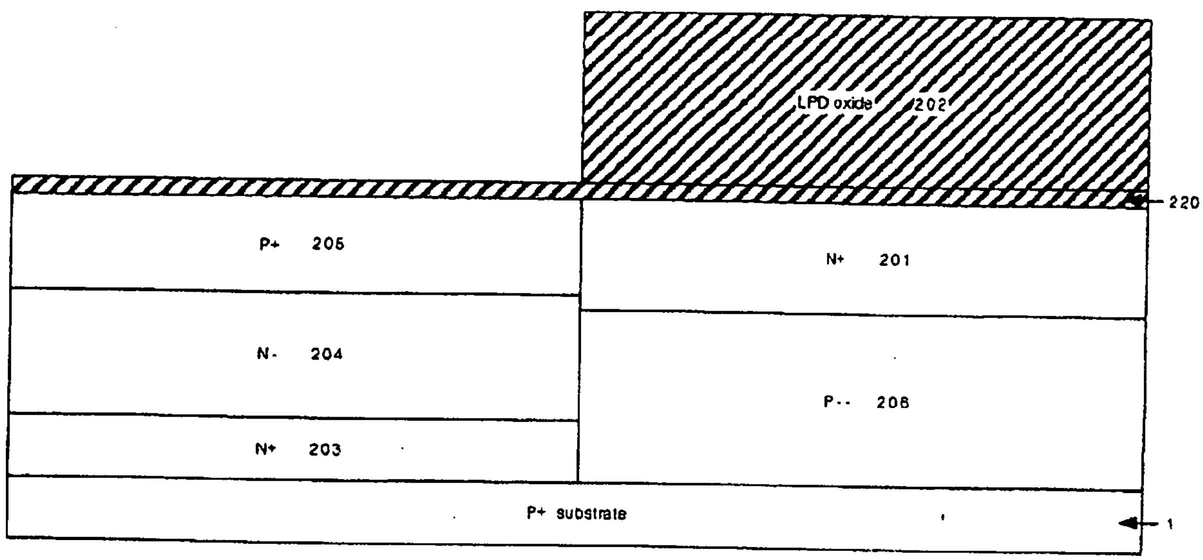
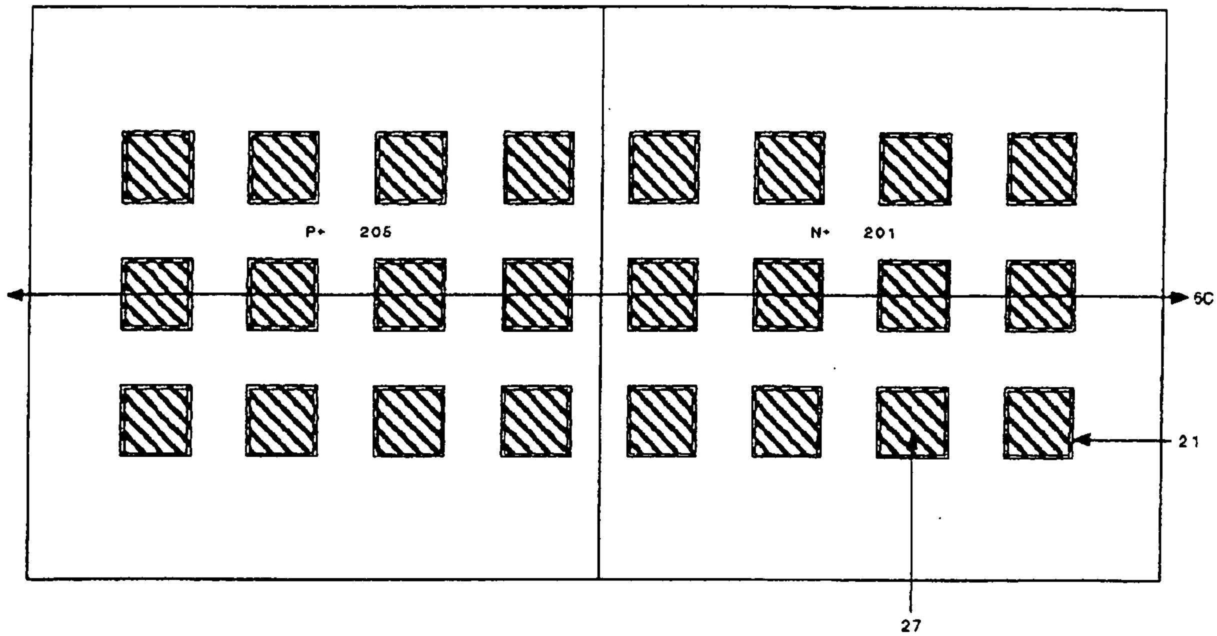
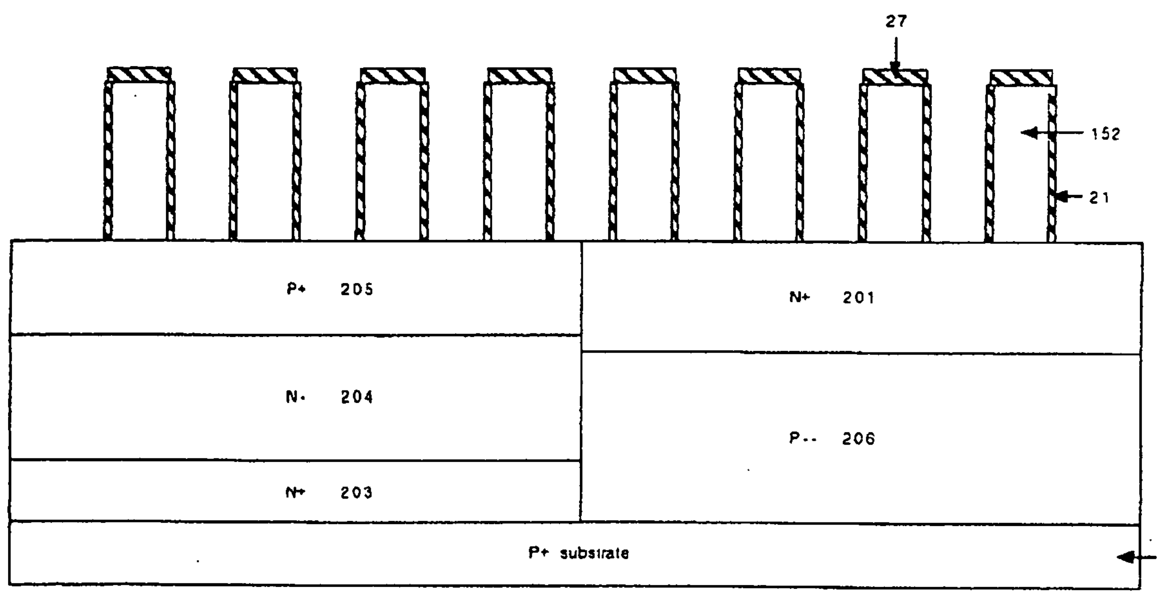

LPD oxide 202
220
P+ 205
N+ 201
N- 204
P-- 206
N+ 203
P+ substrate
1

Fig.6B

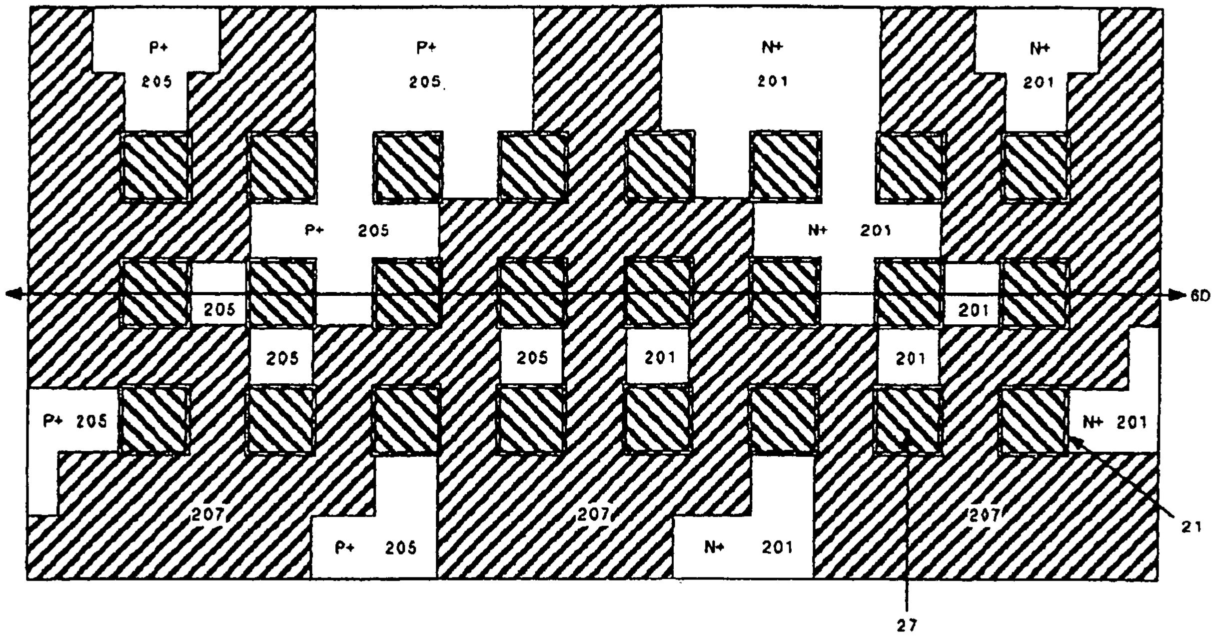


P+ 205
N+ 201
6C
21
27



27
152
21
P+ 205
N+ 201
N- 204
P-- 206
N+ 203
P+ substrate
1

Fig.6C


P+
205
P+
205
N+
201
N+
201
P+ 205
N+ 201
205
201
205
205
201
201
P+ 205
N+ 201
207
207
207
P+ 205
N+ 201
21
27
6D

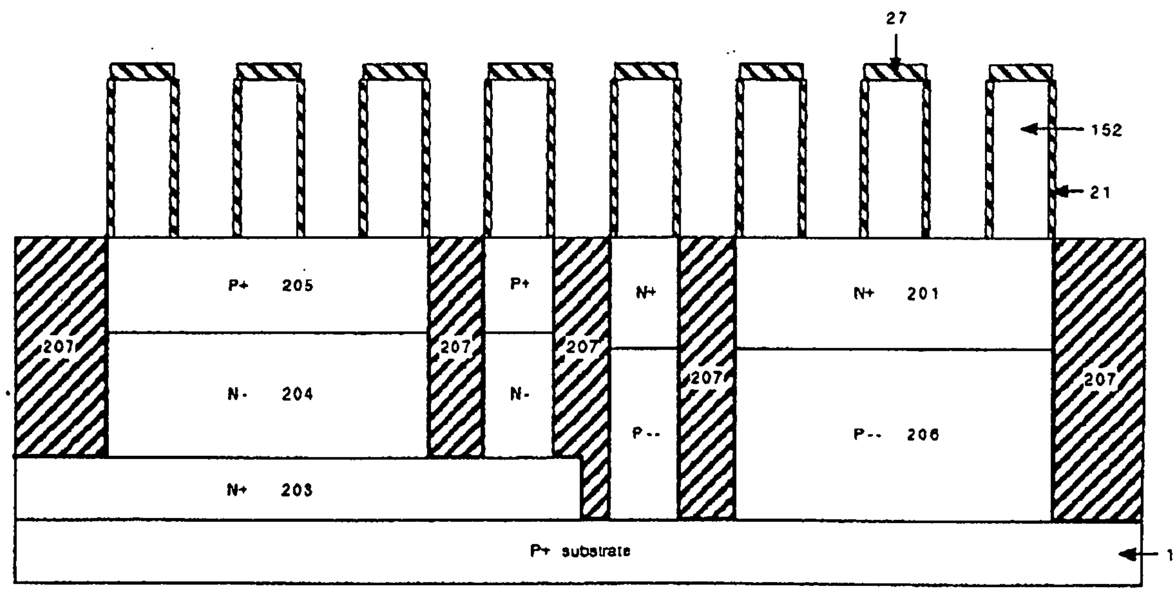
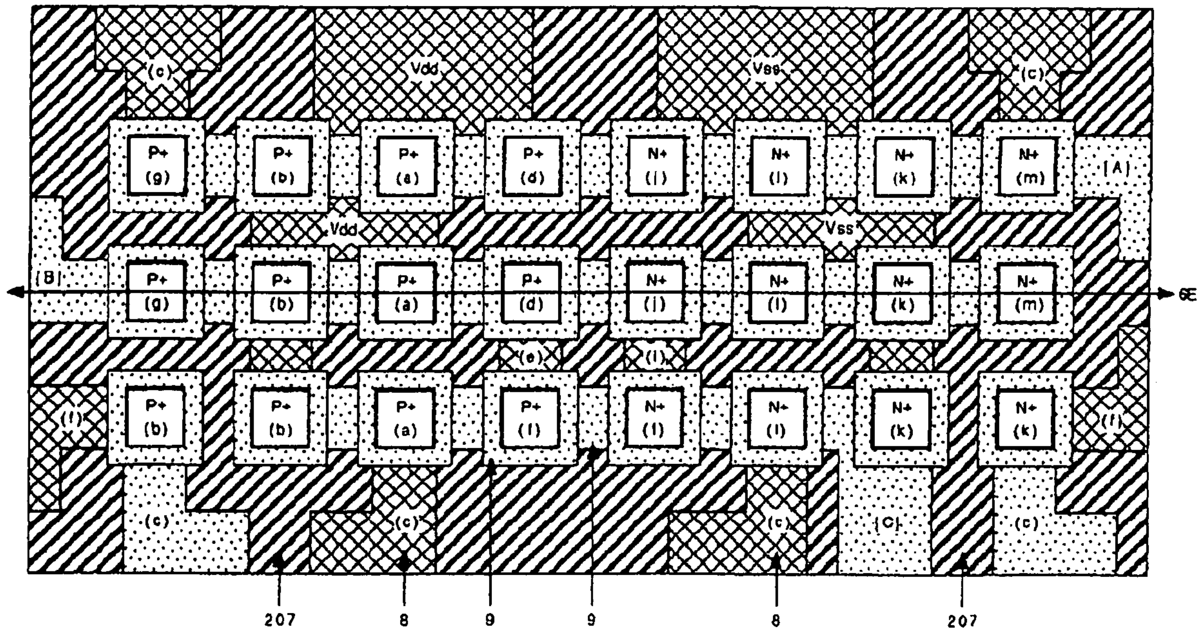

27
152
21
P+ 205
P+
N+
N+ 201
207
207
207
207
207
N- 204
N-
P--
P-- 206
N+ 203
P+ substrate
1

Fig.6D

Logic Circuits (A Full Adder)



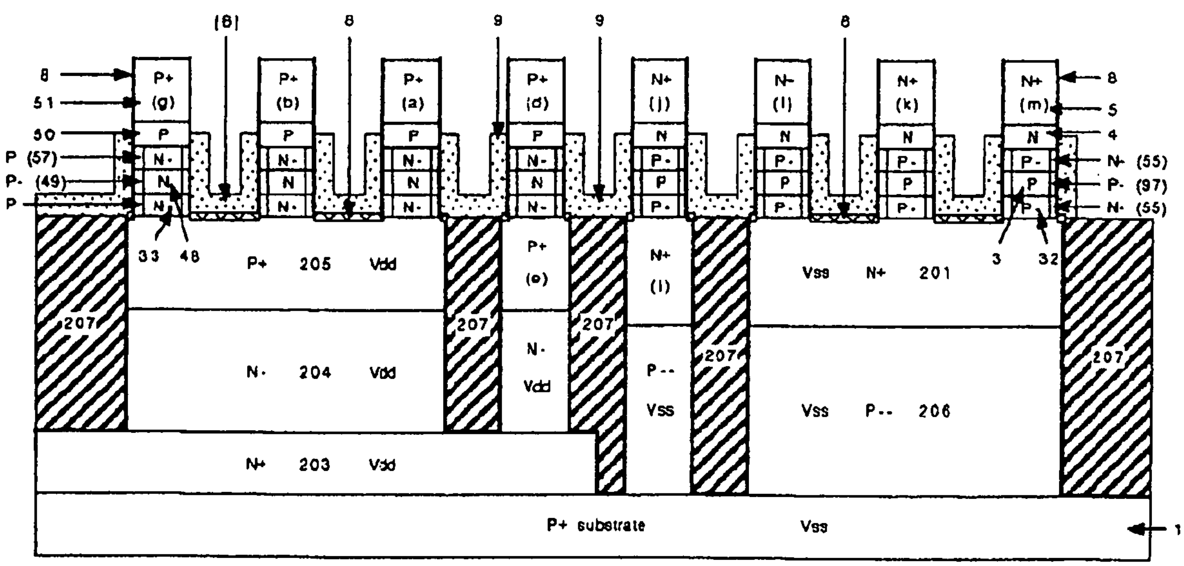
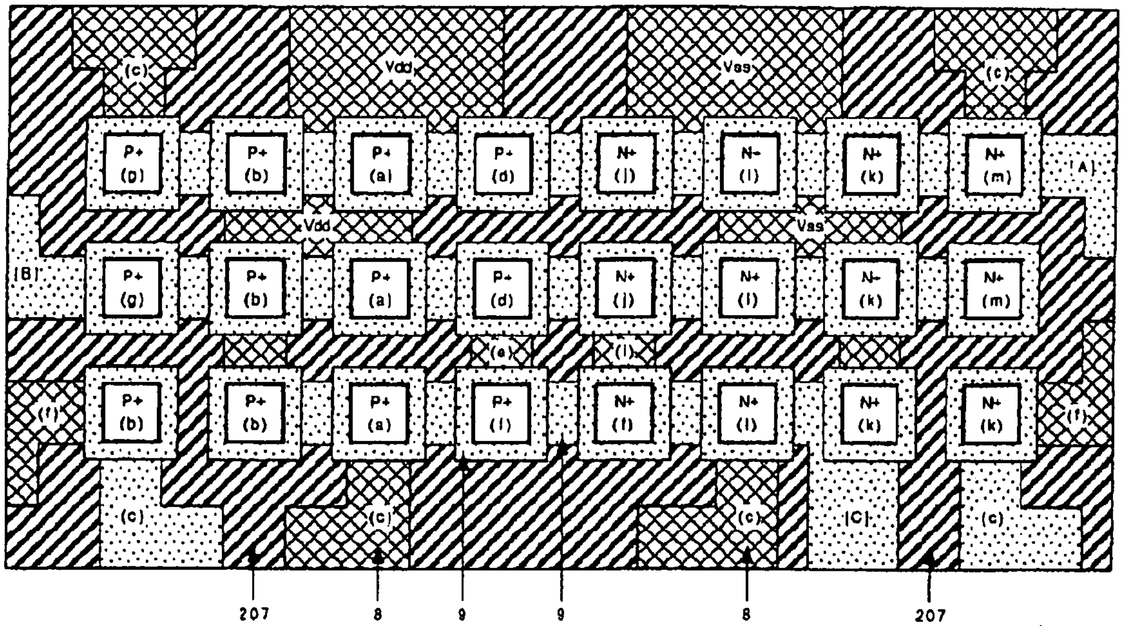


Fig.6E


(c)
Vdd
Vss
(c)
P+ (g)
P+ (b)
P+ (a)
P+ (d)
N+ (j)
N+ (l)
N+ (k)
N+ (m)
(A)
Vdd
Vss
(B)
(e)
(i)
(f)
P+ (b)
P+ (a)
P+ (f)
N+ (f)
N+ (k)
(f)
(c)
(c)
(c)
(C)
(c)
207
8
9
9
8
207

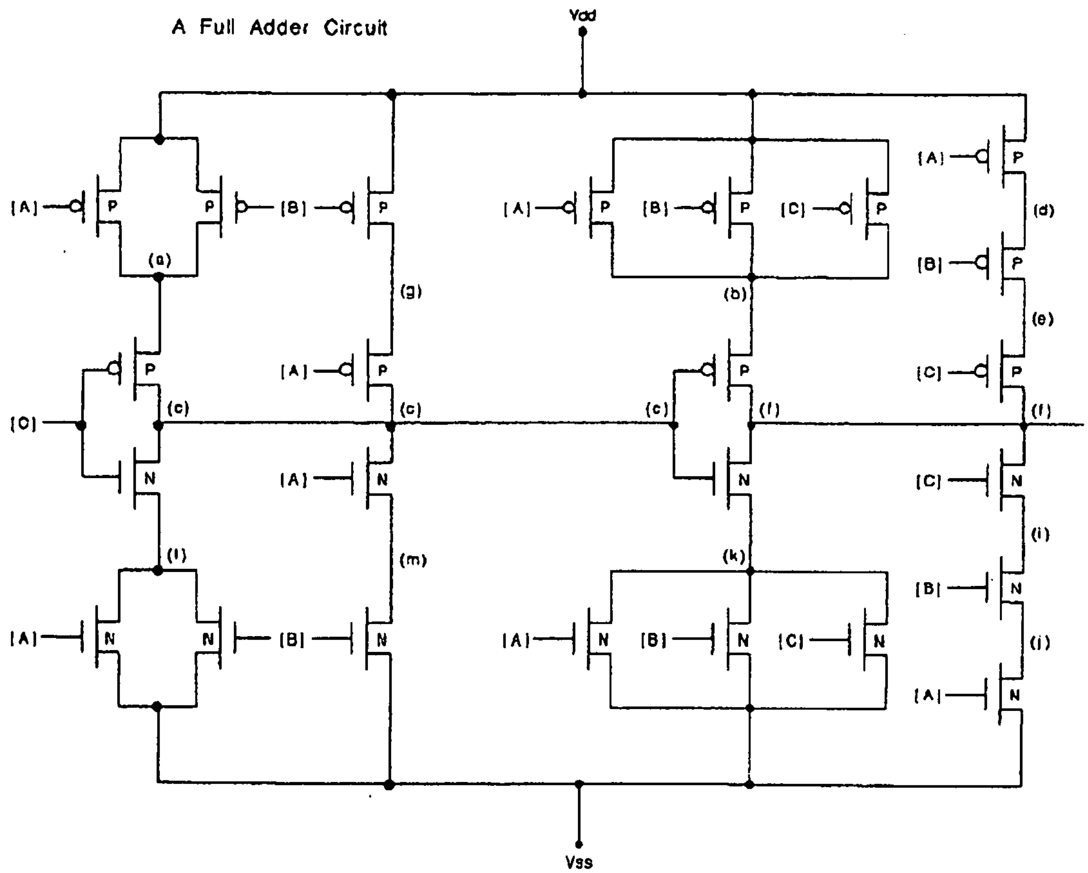
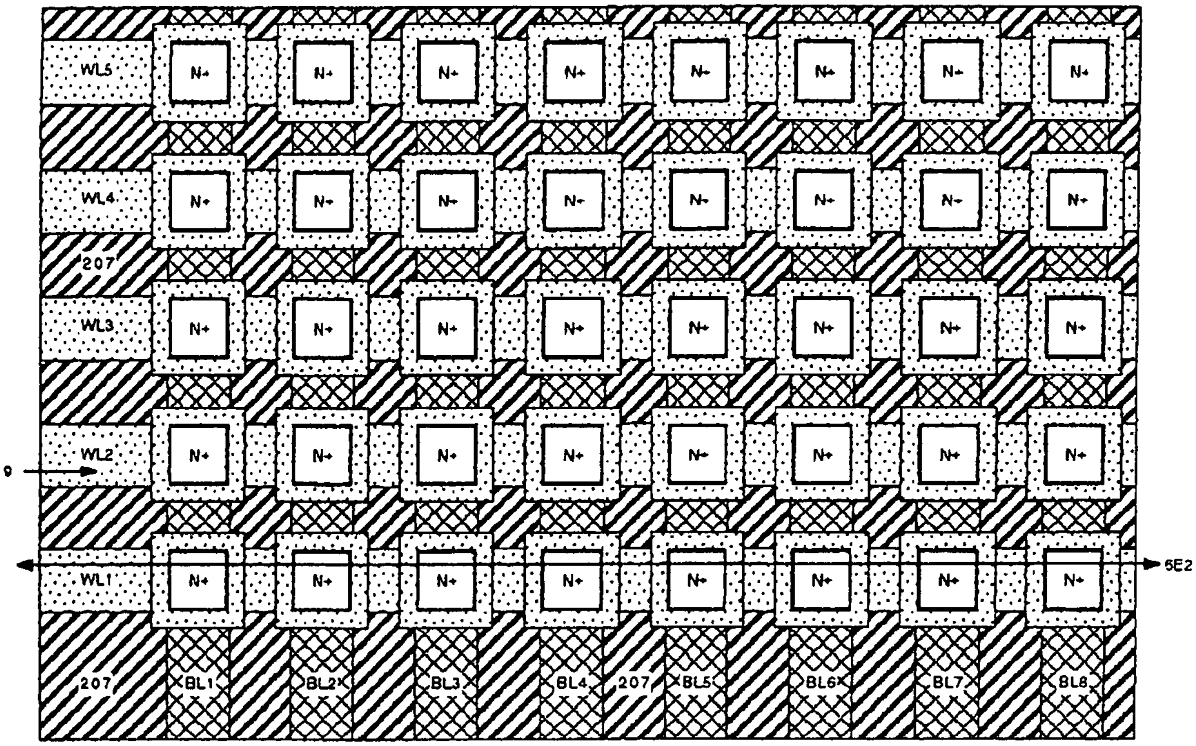

A Full Adder Circuit
Vdd
Vss
(A)
(B)
(C)
(a)
(b)
(c)
(d)
(e)
(f)
(g)
(i)
(j)
(k)
(l)
(m)
P
N

Fig.6E1

Memory Array (DRAM)



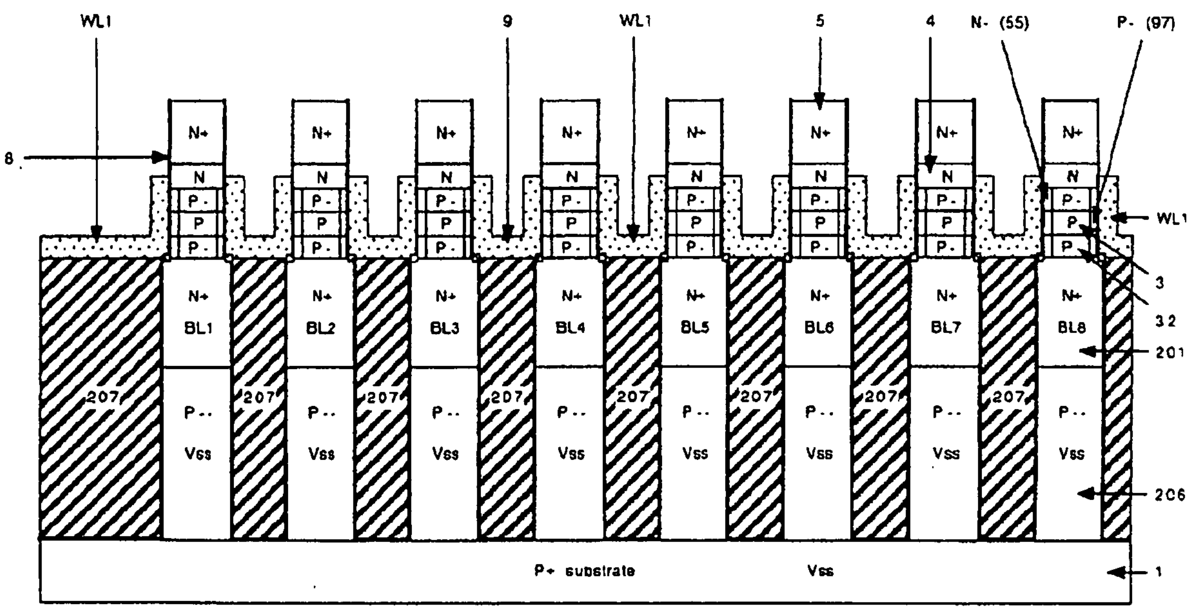
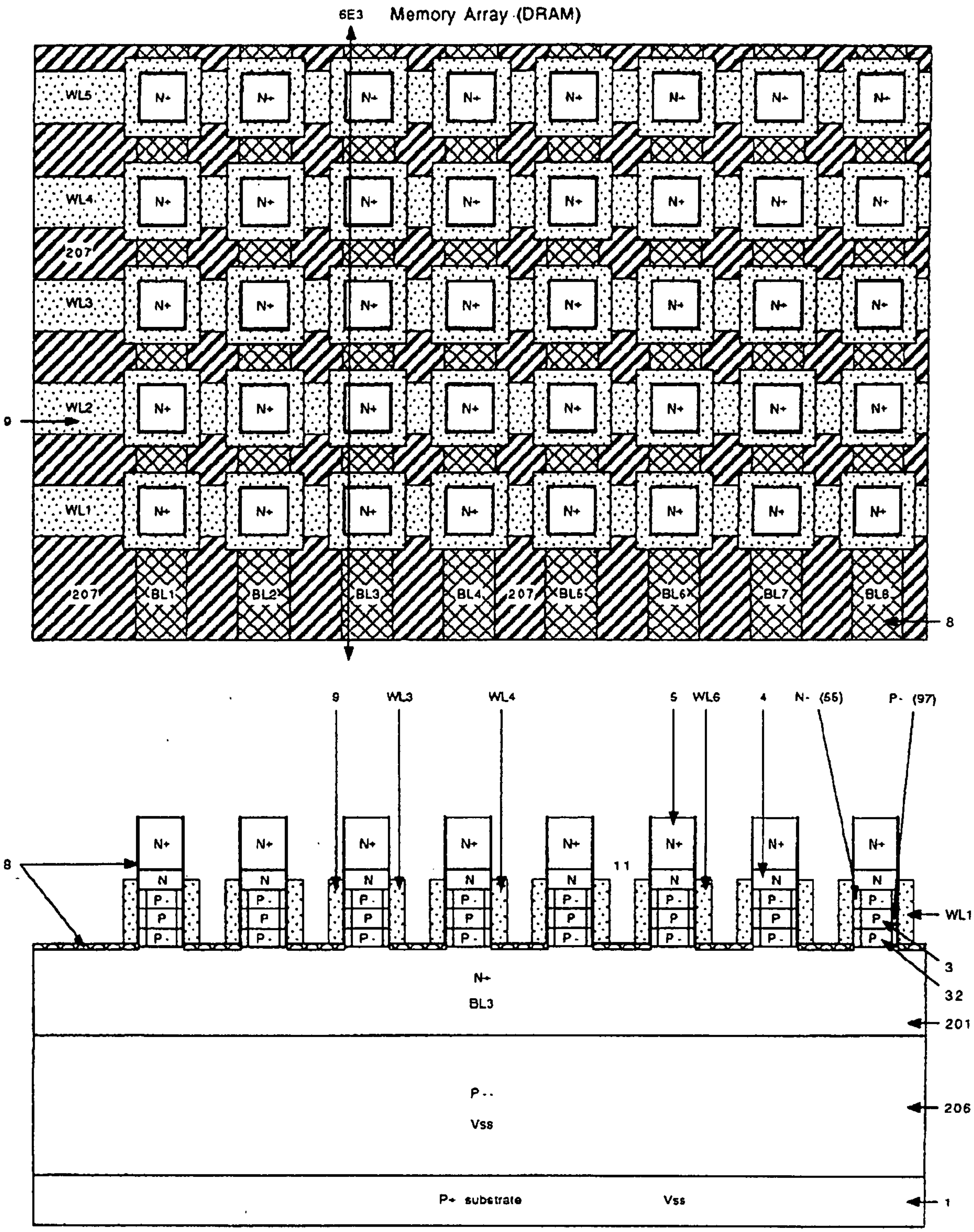


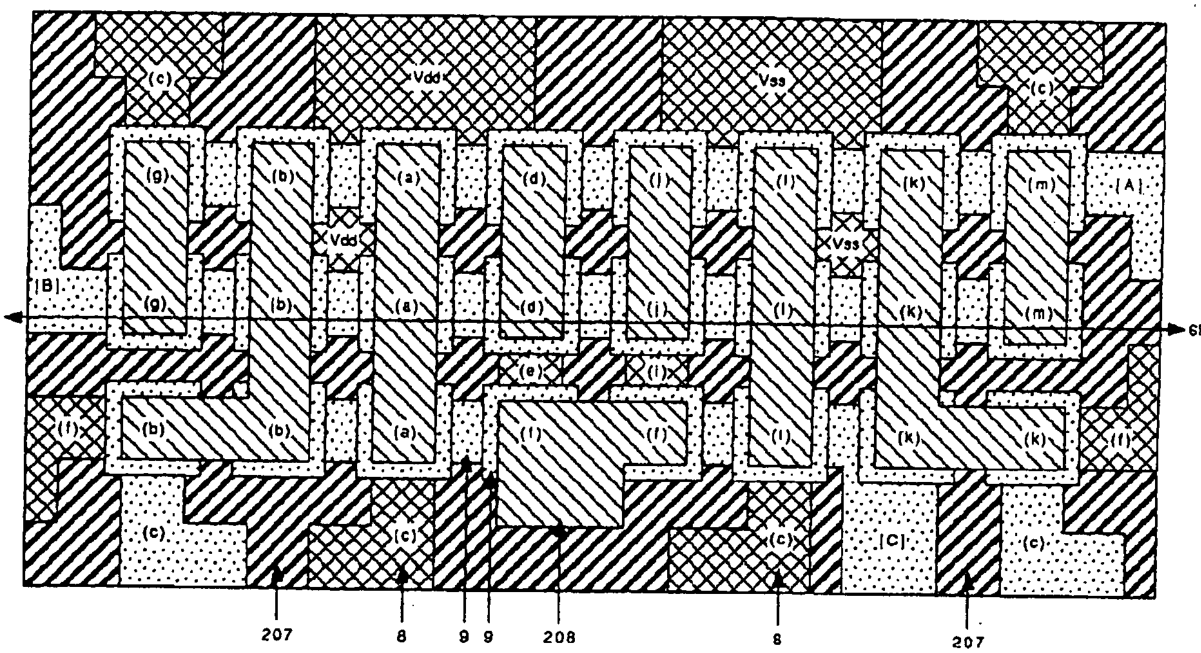
Fig.6E2



6E3
Memory Array (DRAM)
WL5
WL4
WL3
WL2
WL1
207
9
N+
BL1
BL2
BL3
BL4
BL5
BL6
BL7
BL8
8
9
WL3
WL4
5
WL6
4
N- (55)
P- (97)
N
P-
P
11
WL1
3
32
BL3
201
P--
Vss
206
P+ substrate
1

Fig.6E3

Logic Circuits (A Full Adder)



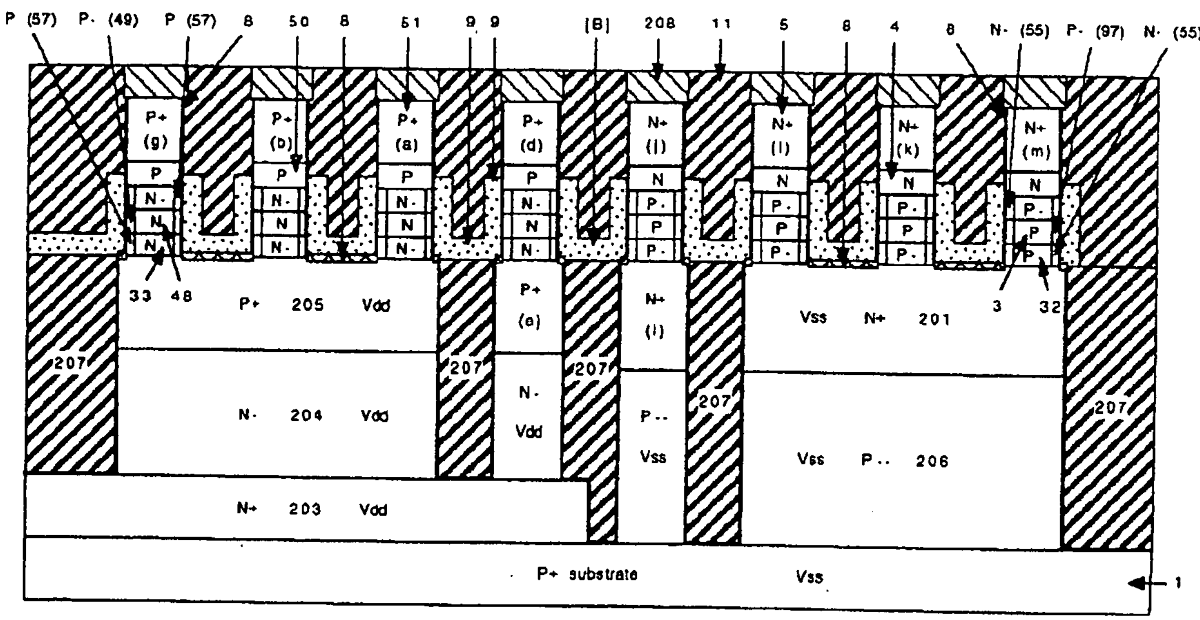


Fig.6F

Logic Circuits (A Full Adder)

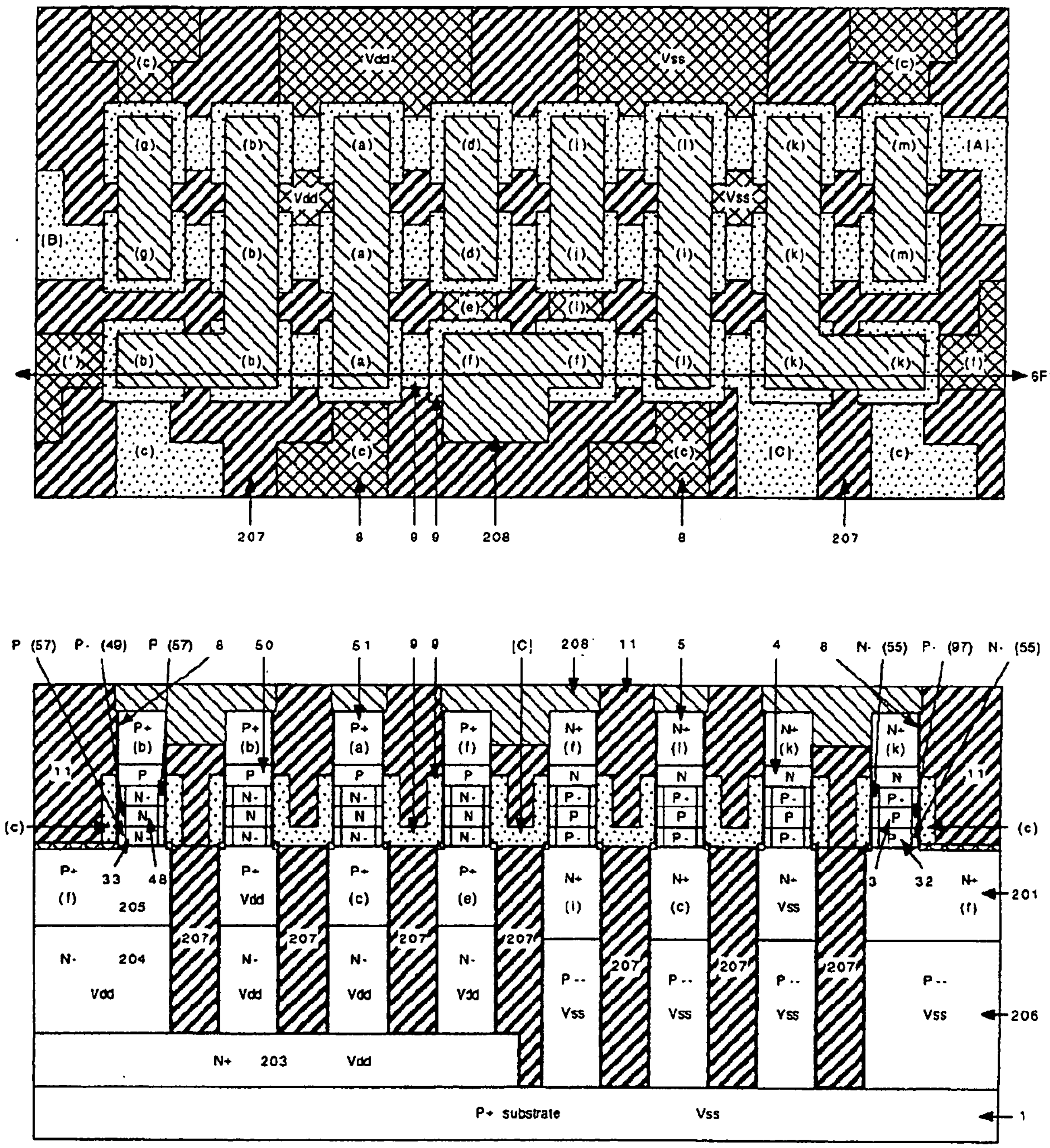
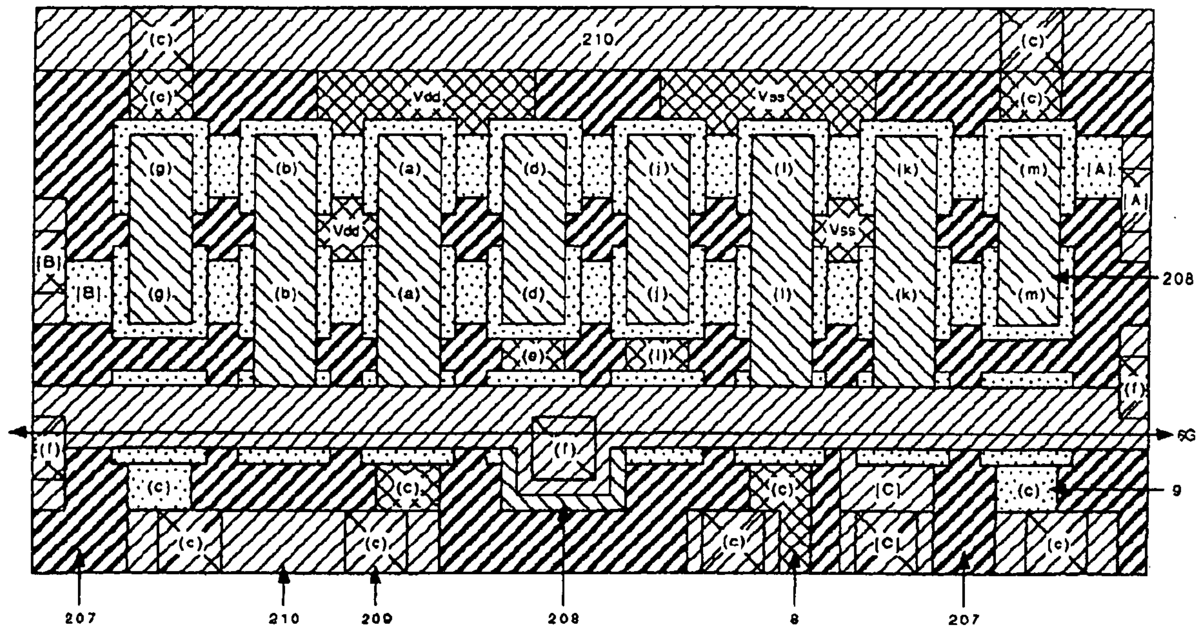


Fig.6F1

Logic Circuits (A Full Adder)



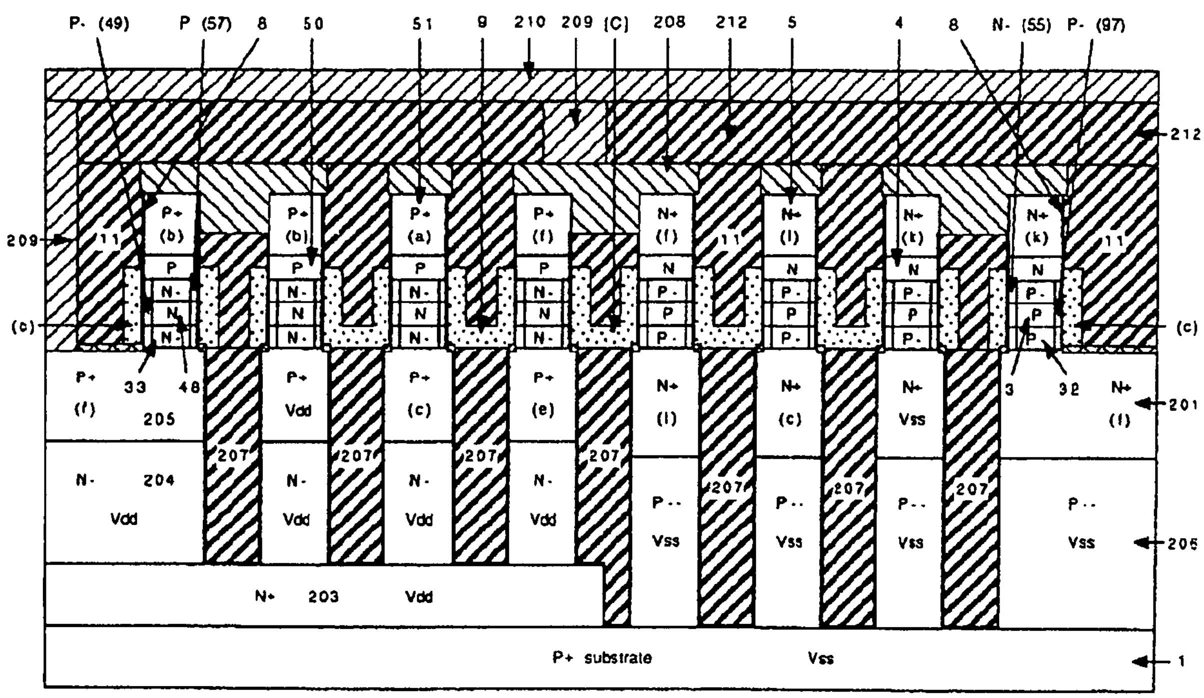
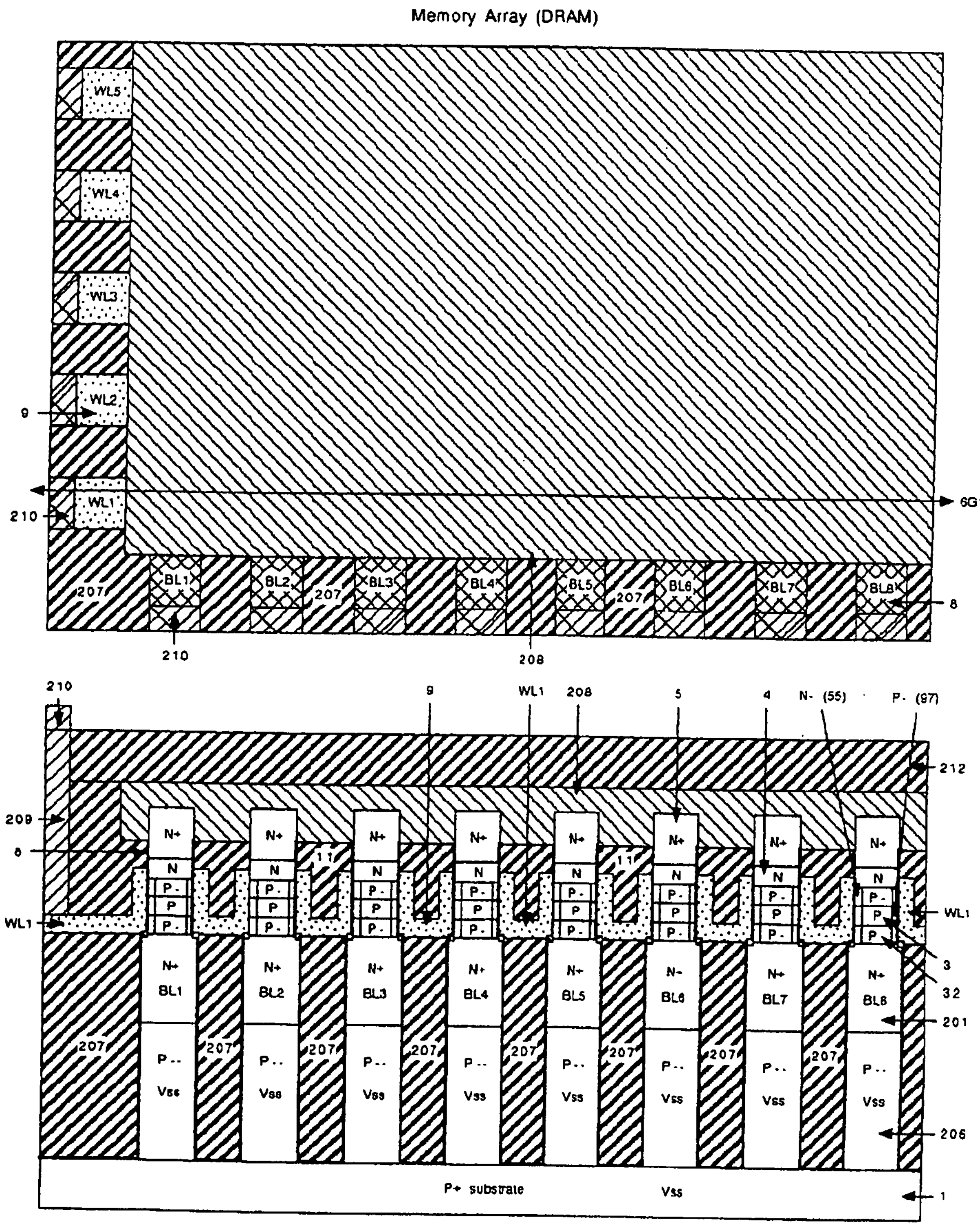
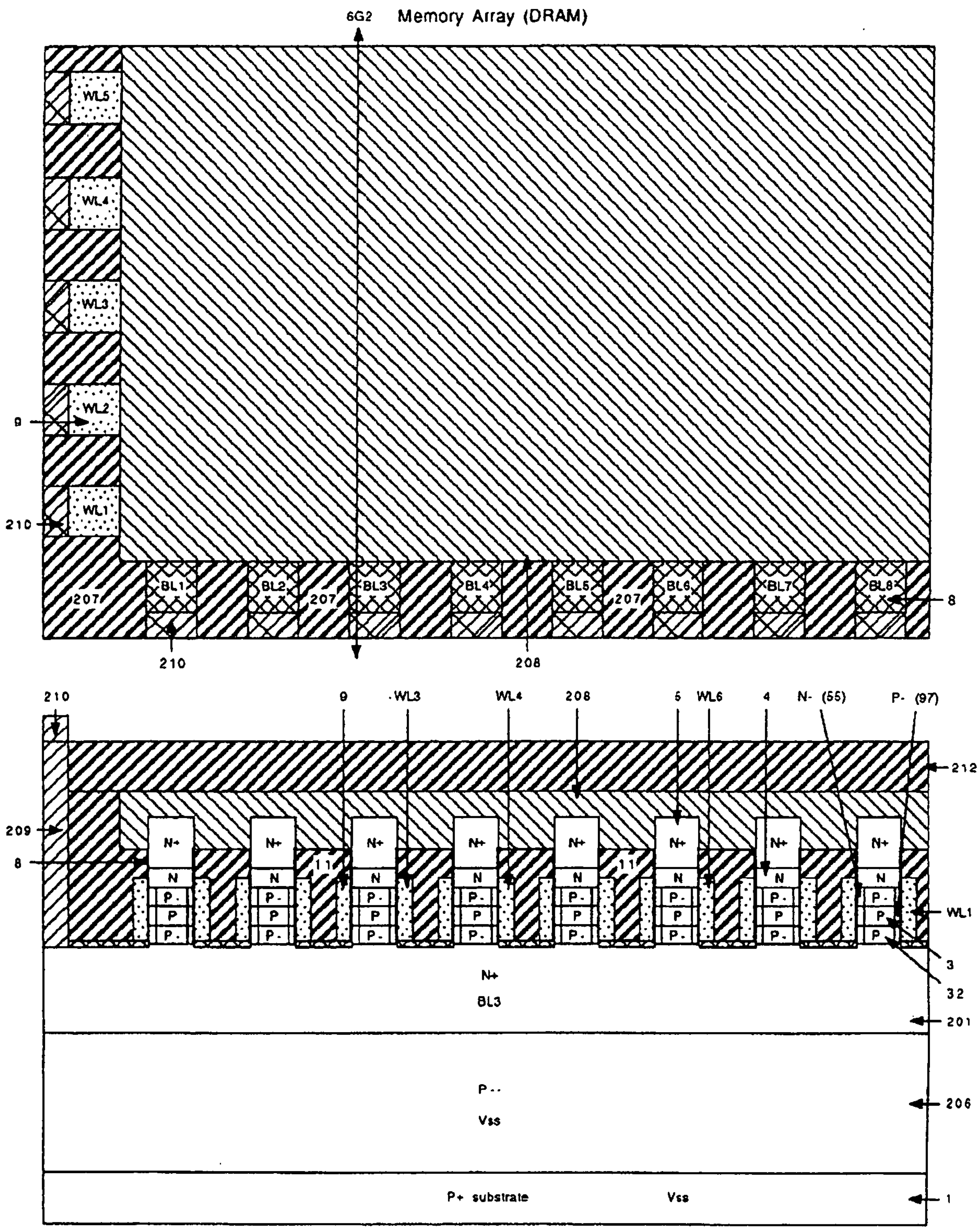


Fig.6G



Memory Array (DRAM)
WL5
WL4
WL3
WL2
WL1
9
210
6G1
207
BL1
BL2
BL3
BL4
BL5
BL6
BL7
BL8
8
208
212
209
N- (55)
P- (97)
5
4
11
N+
N
P-
P
BL1
BL2
BL3
BL4
BL5
BL6
BL7
BL8
P--
Vss
3
32
201
206
P+ substrate
1

Fig.6G1



6G2
Memory Array (DRAM)
WL5
WL4
WL3
WL2
WL1
9
210
207
BL1
BL2
BL3
BL4
BL5
BL6
BL7
BL8
8
208
WL3
WL4
5
WL6
4
N- (55)
P- (97)
212
209
N+
N
P-
P
11
WL1
3
32
BL3
201
P--
Vss
206
P+ substrate
1

Fig.6G2

Logic Circuits (A Full Adder)

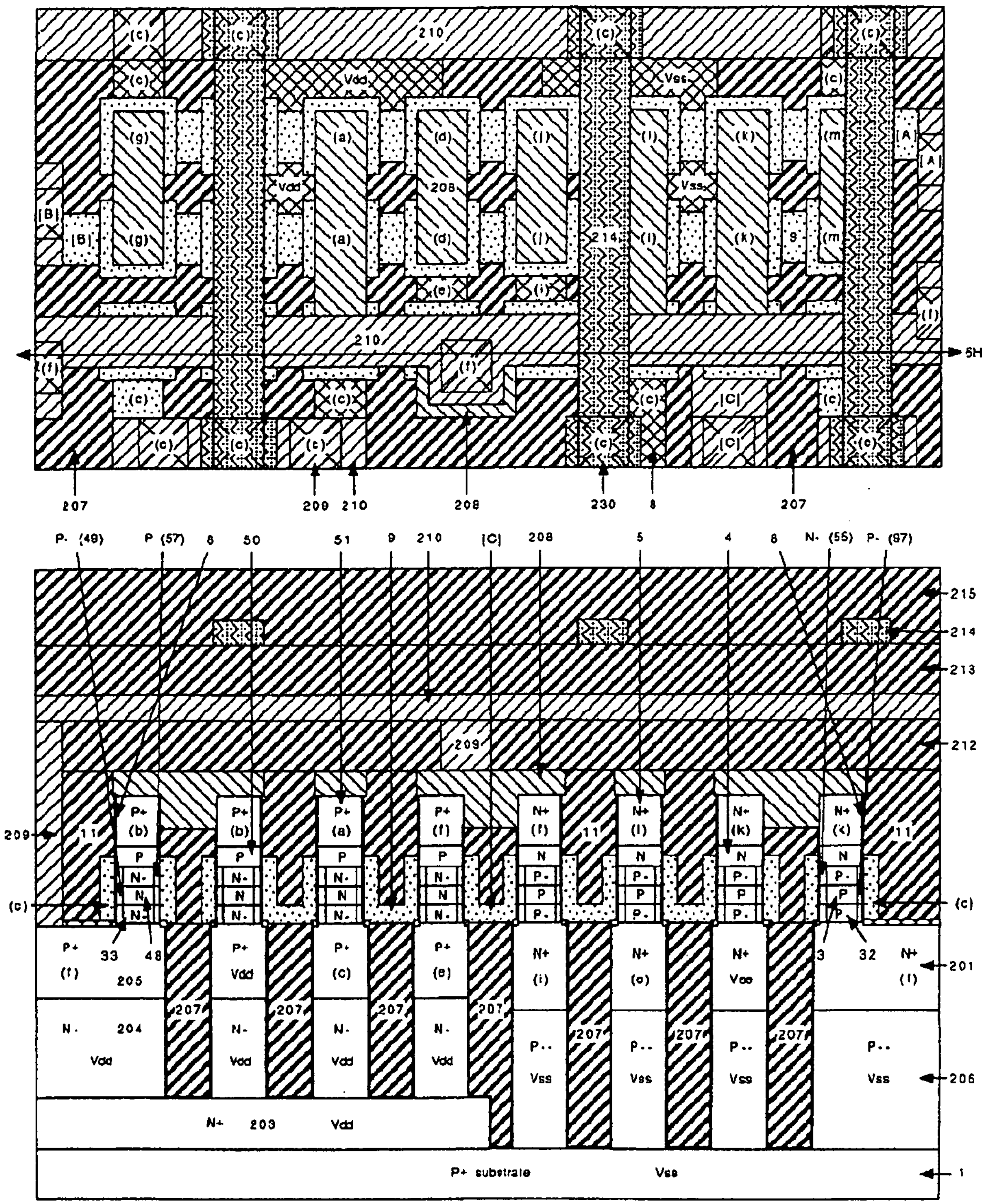


Fig.6H

Memory Array (DRAM)

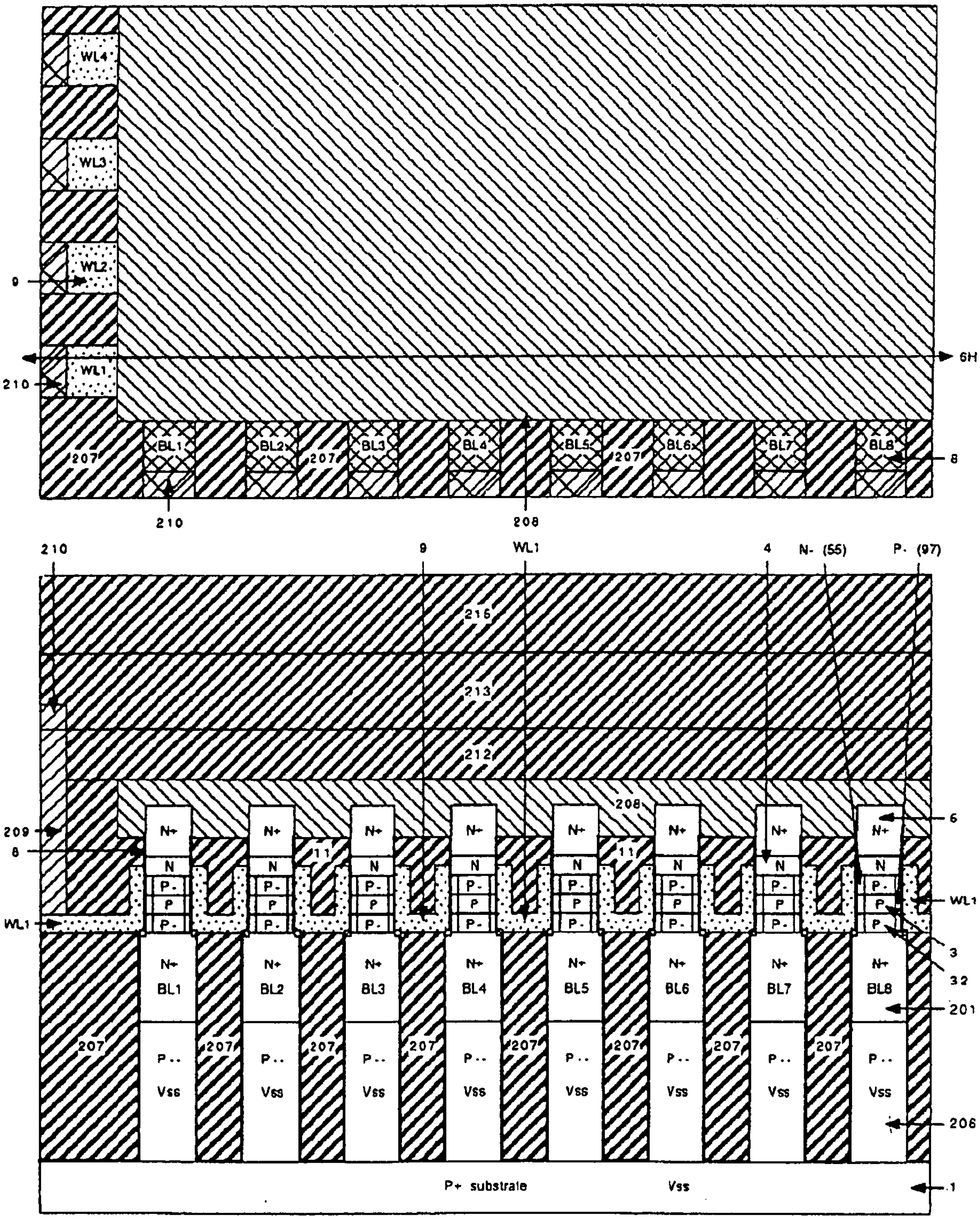


Fig.6H1

Memory Array (DRAM)

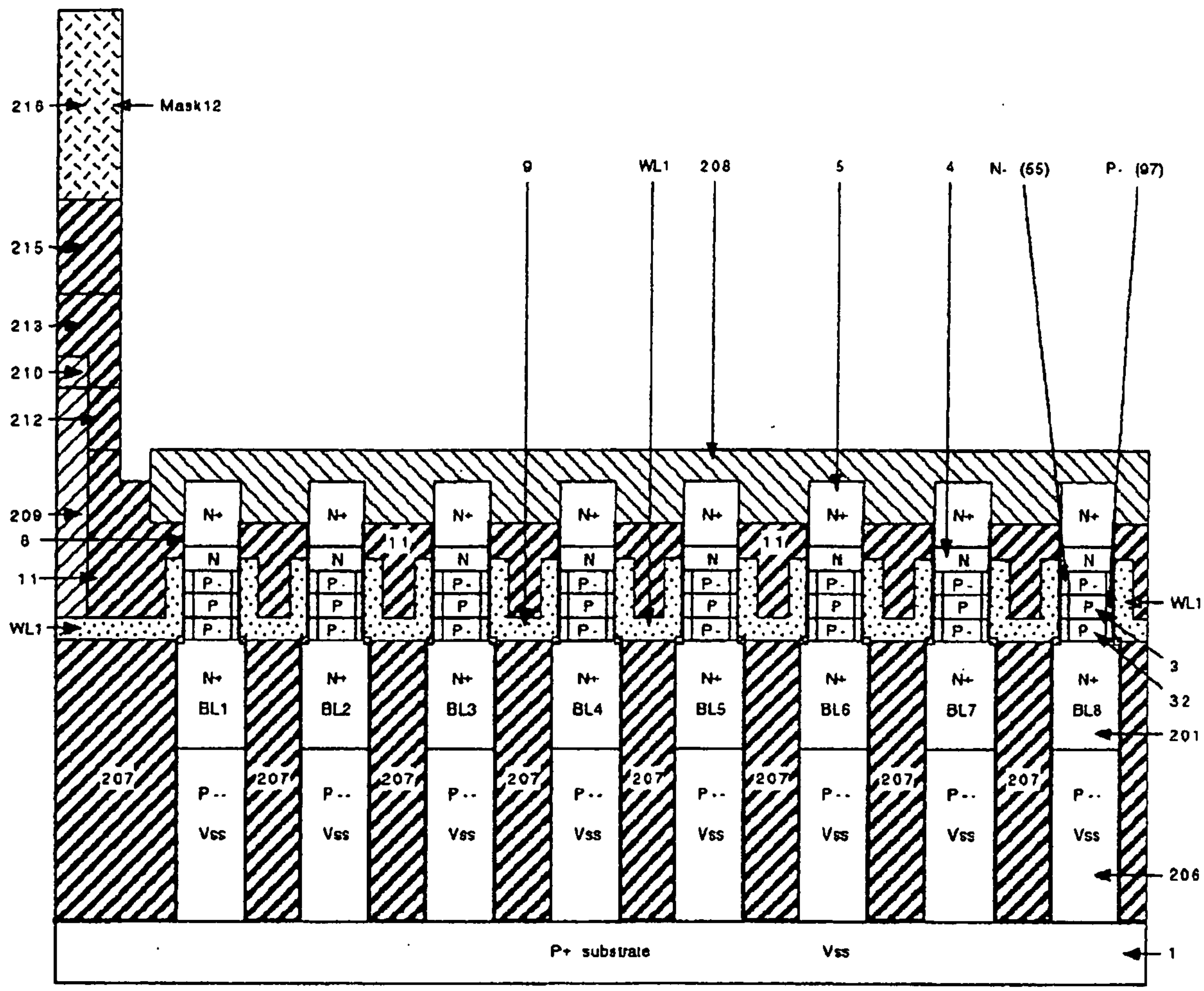


Fig.6I

Memory Array (DRAM)

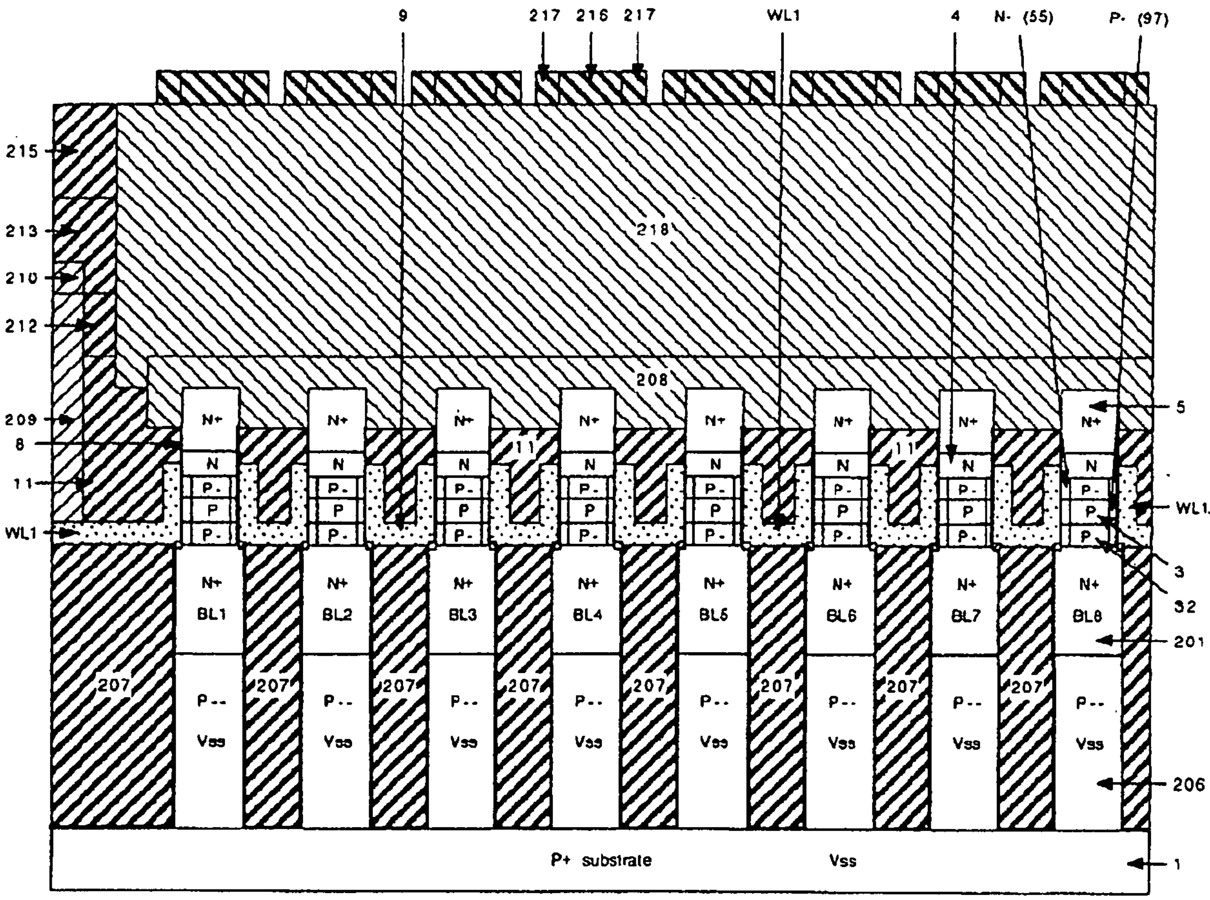


Fig.6J

Memory Array (DRAM)

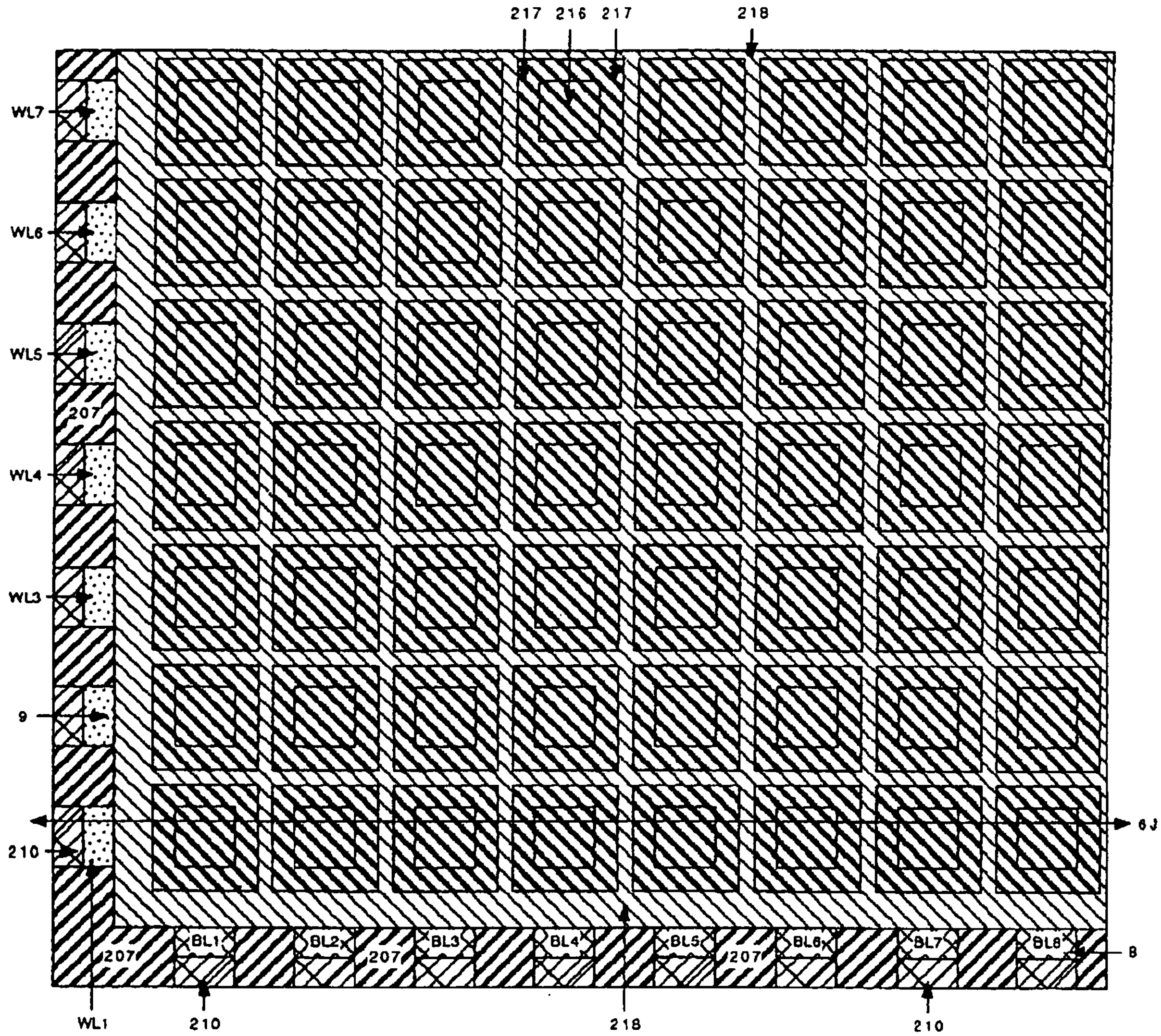


Fig.6J1

Memory Array (DRAM)

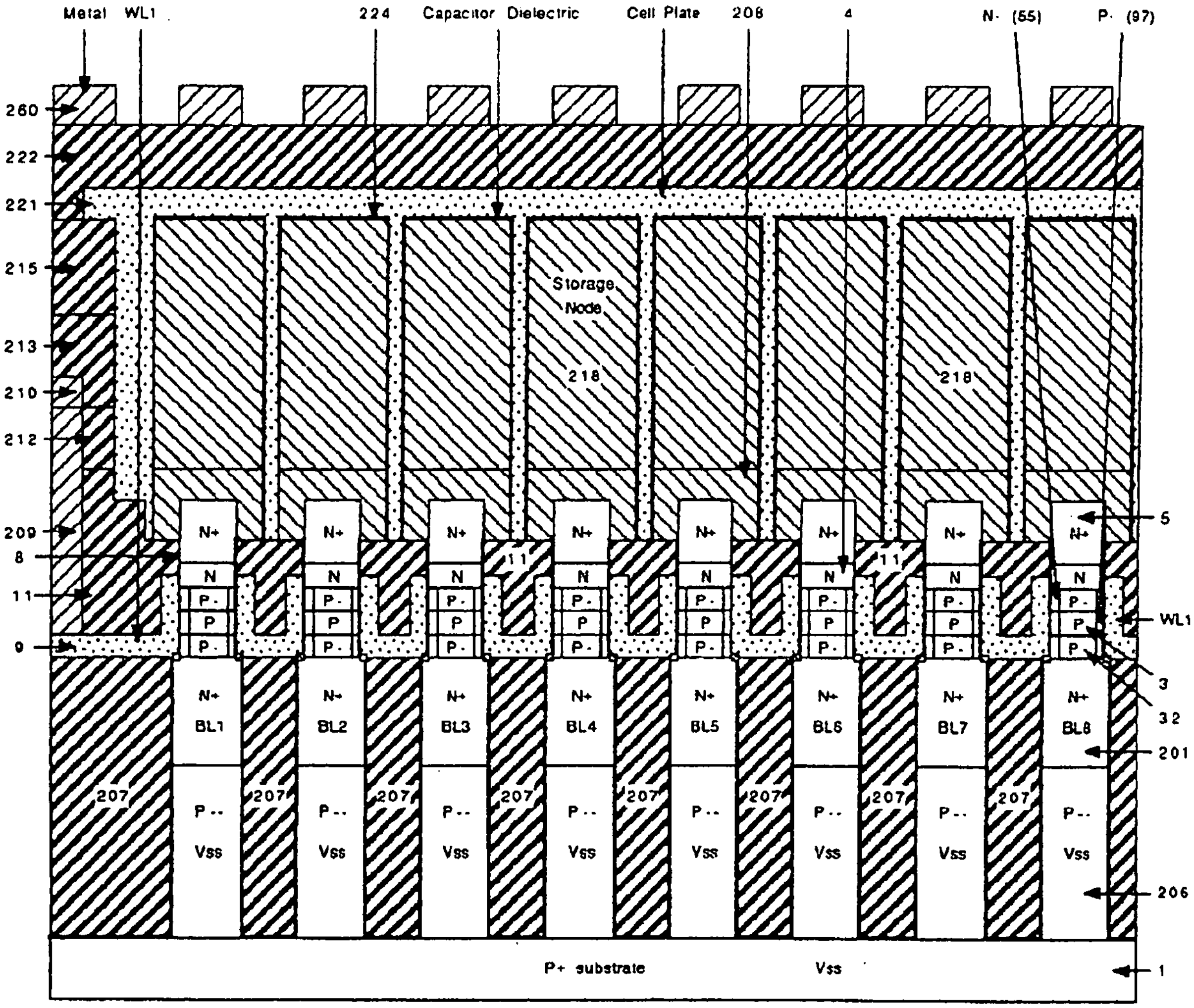


Fig.6K

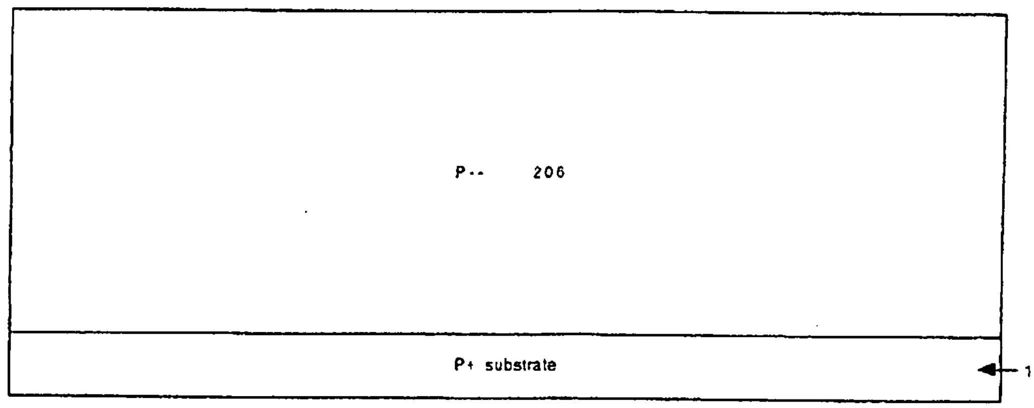

P-- 206
P+ substrate
1

Fig.7A

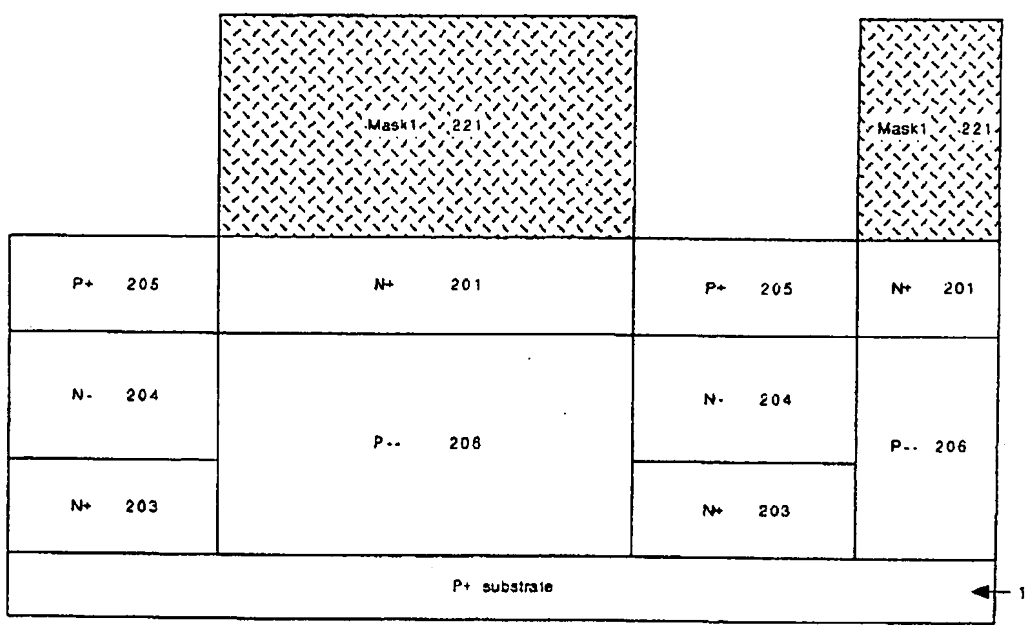

Mask1 221
Mask1 221
P+ 205
N+ 201
P+ 205
N+ 201
N- 204
P-- 206
N- 204
P-- 206
N+ 203
N+ 203
P+ substrate
1

Fig.7B

Memory Array (SRAM)

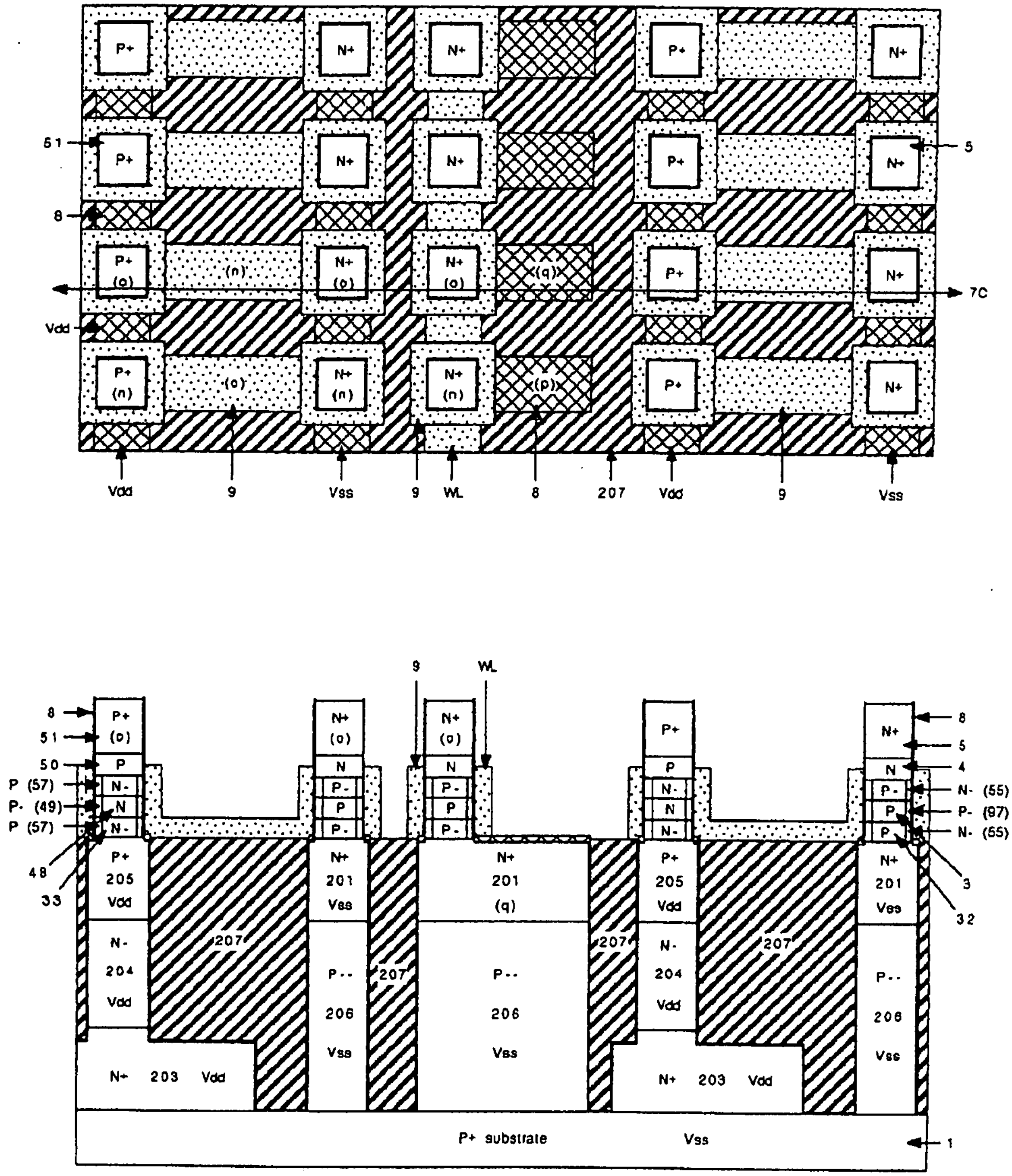
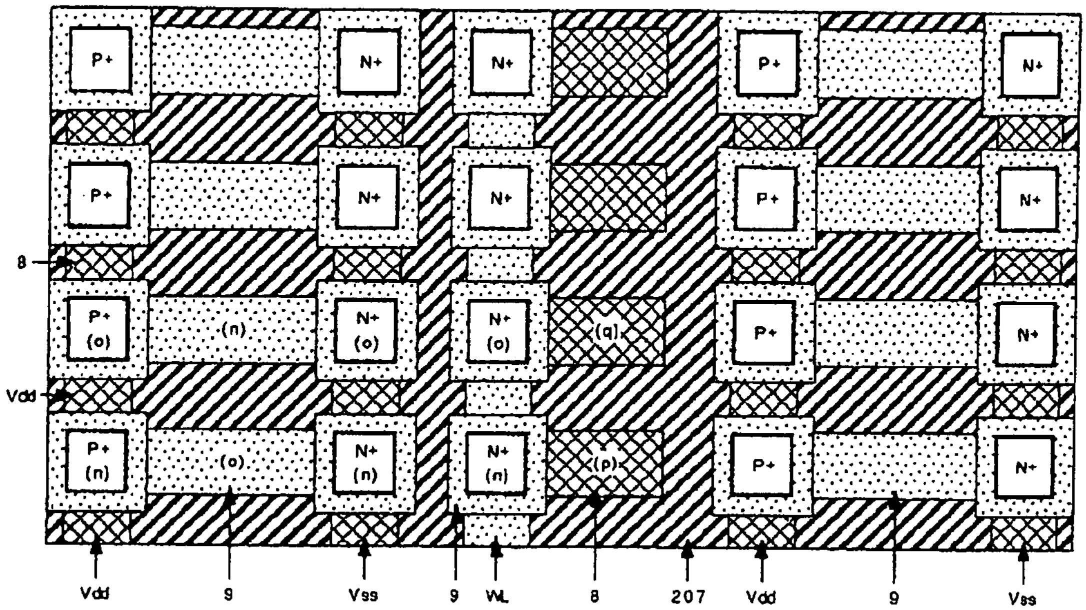


Fig.7C

Memory Array (SRAM)



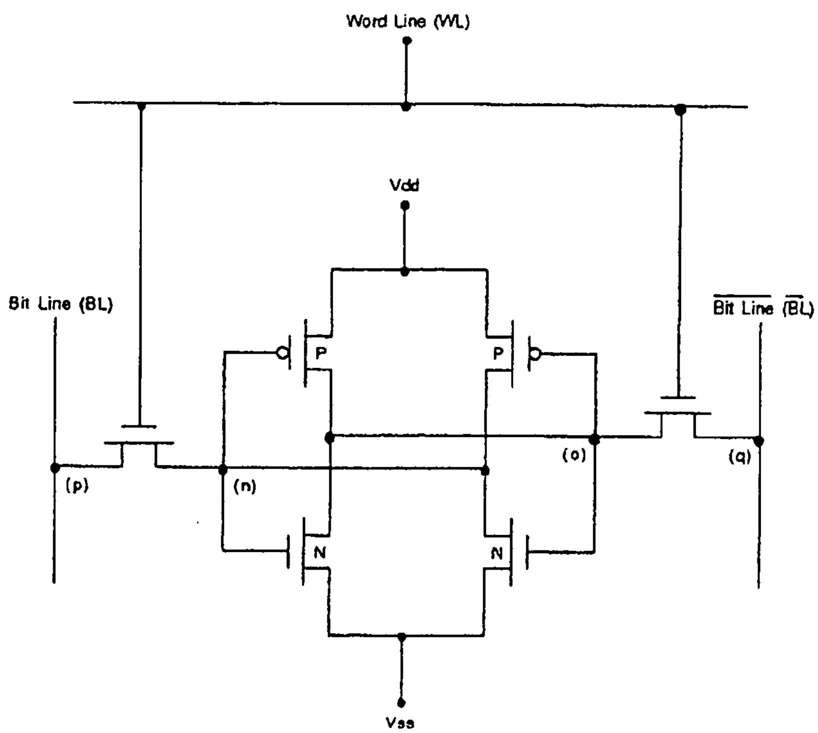


Fig.7C1

Logic Circuits (A Full Adder)

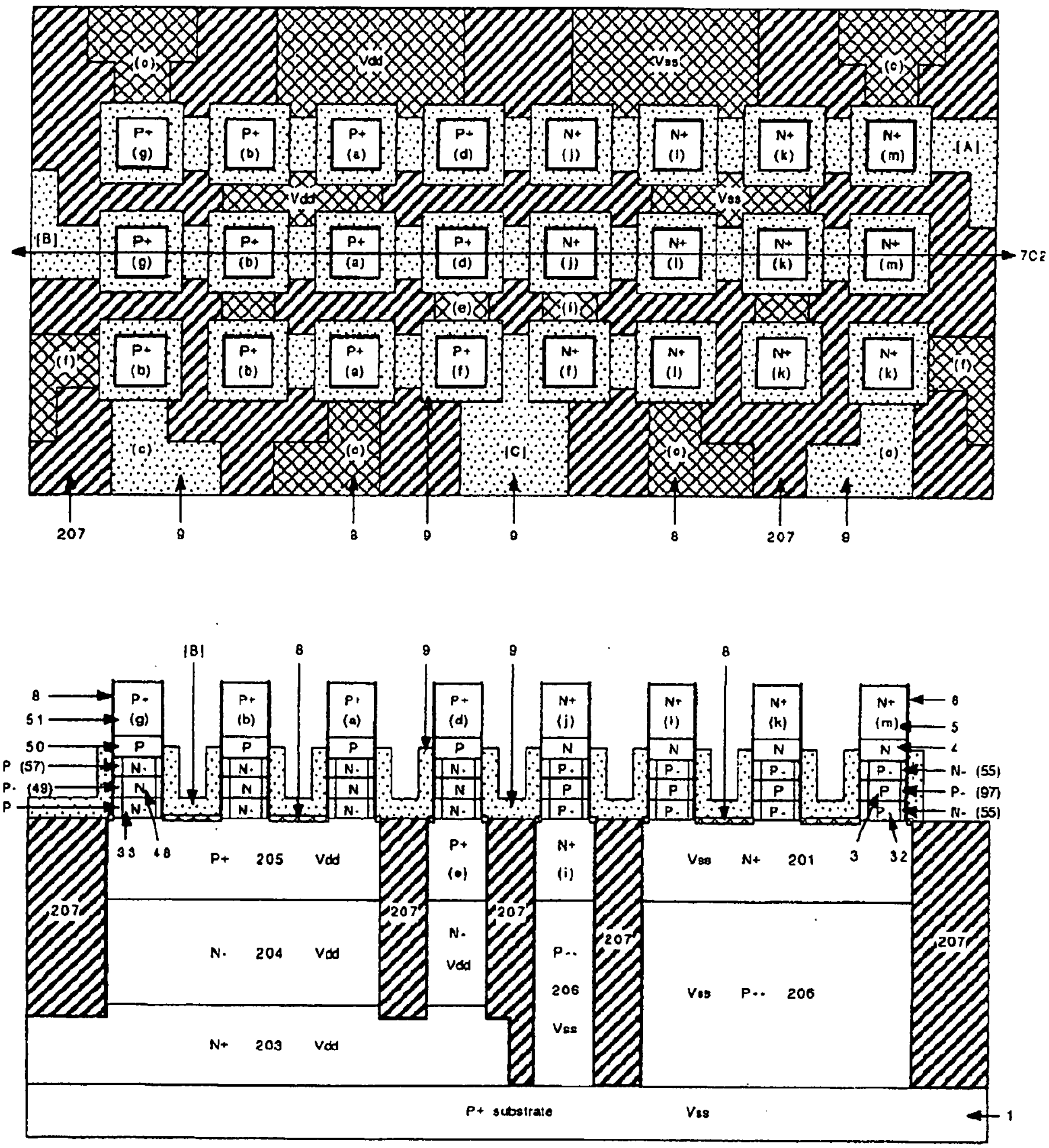
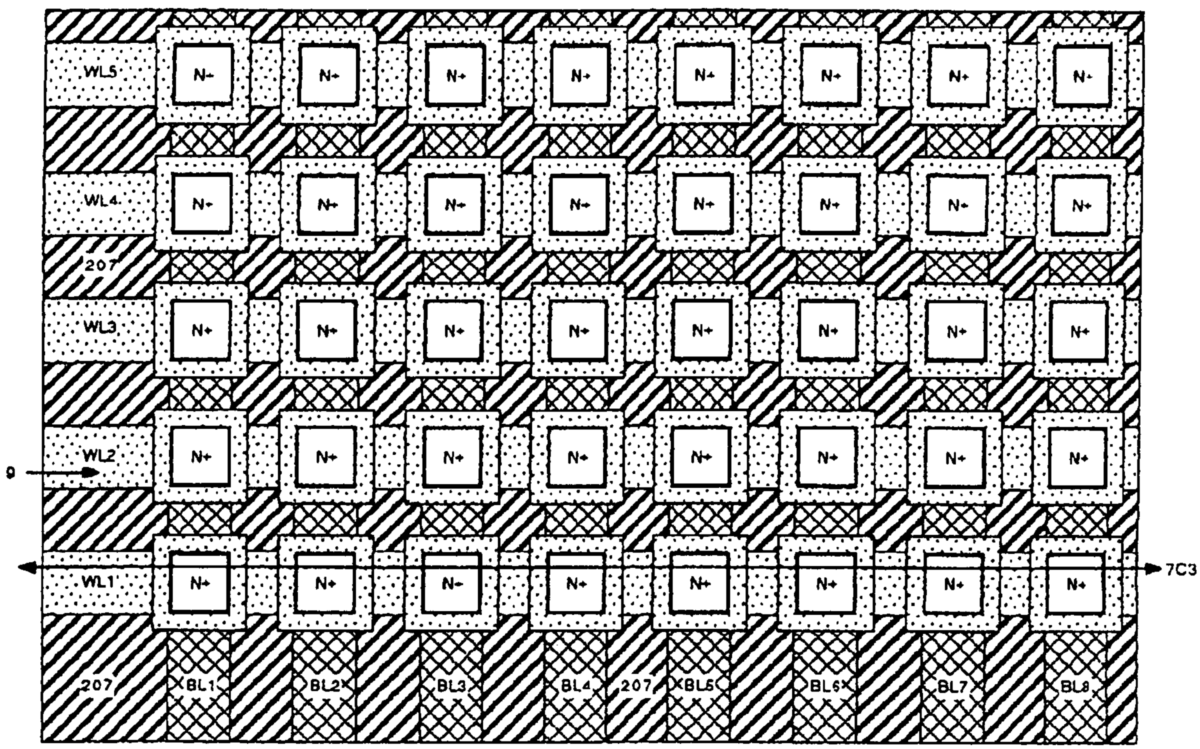


Fig.7C2

Memory Array (DRAM)



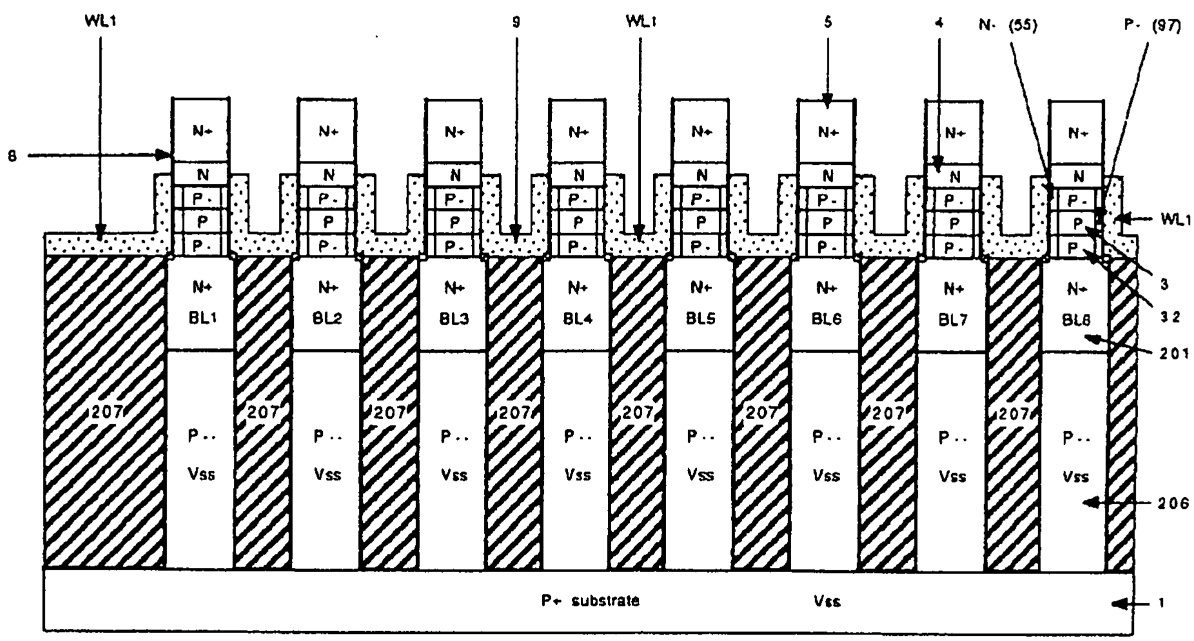


Fig.7C3

Logic circuits (CMOS flip-flop)

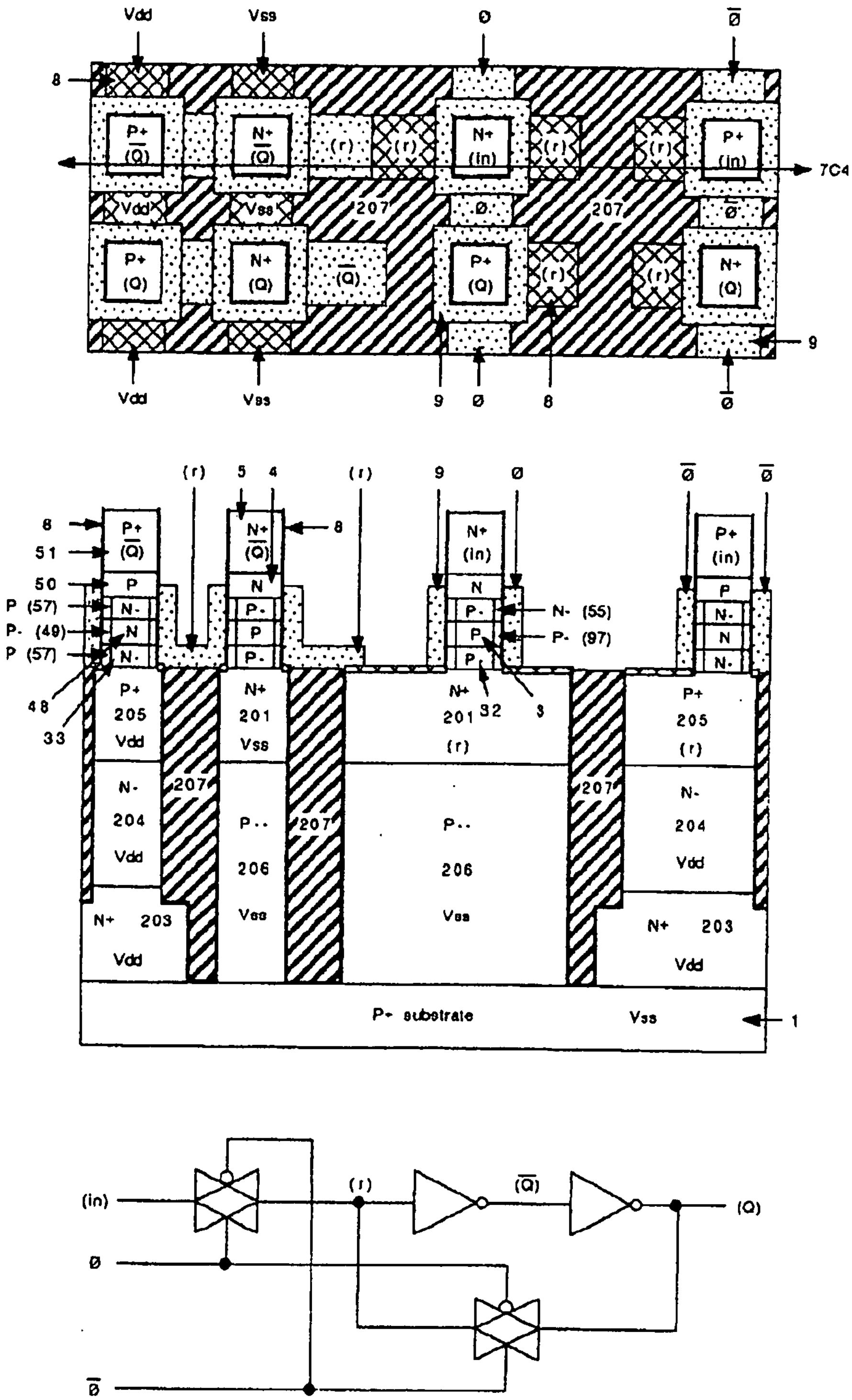


Fig.7C4

Logic circuits (CMOS flip-flop)

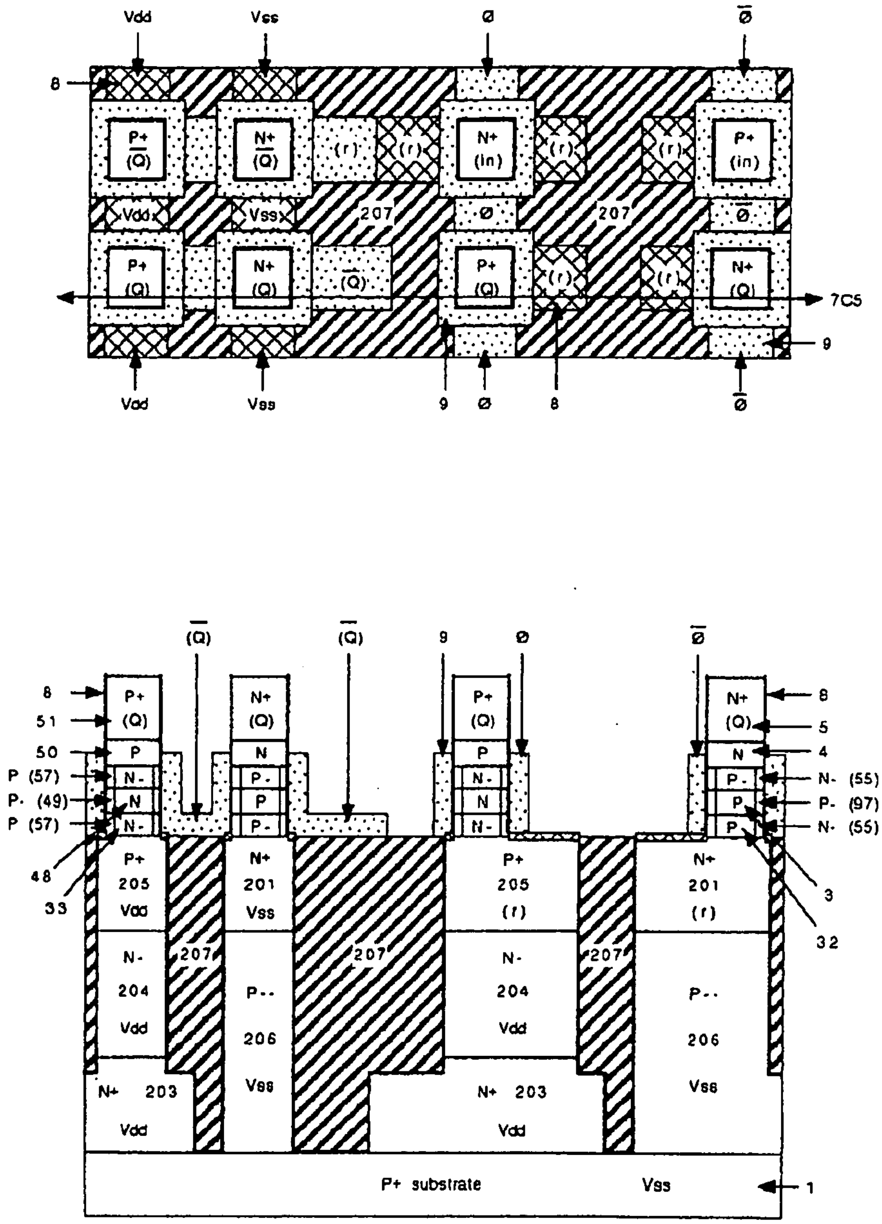


Fig.7C5

Logic circuits (CMOS NAND)

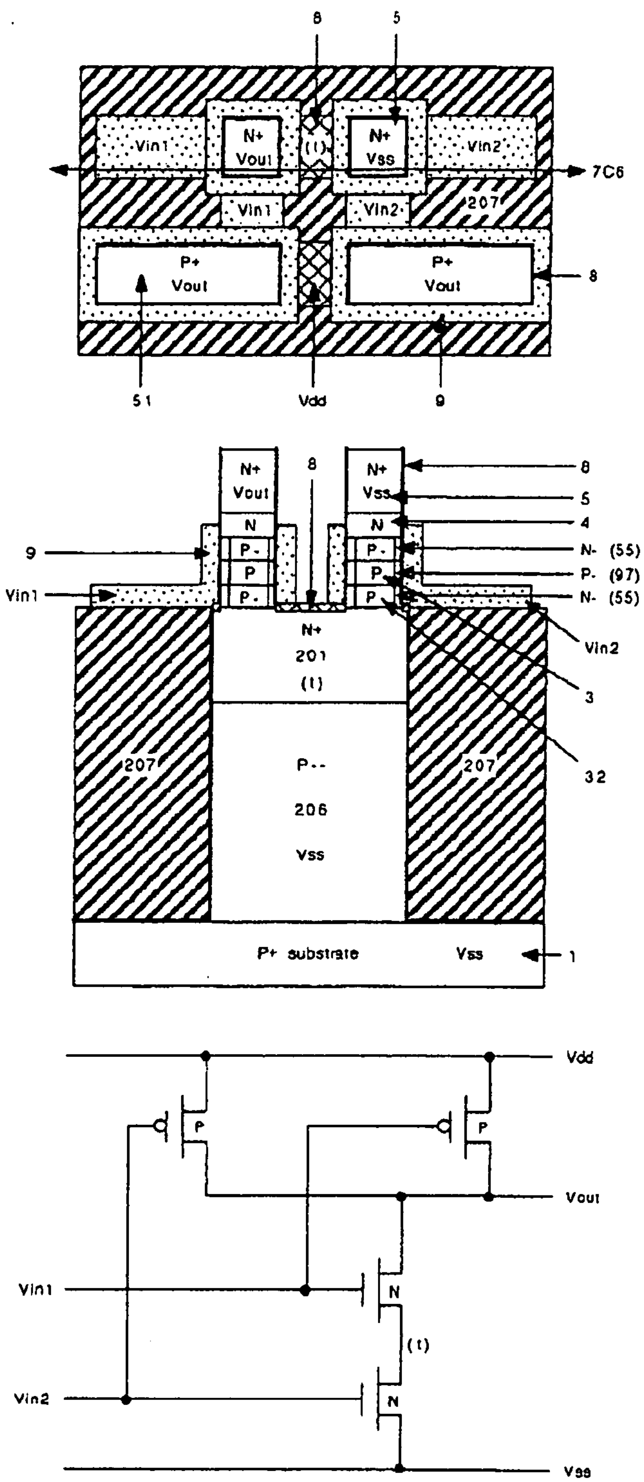
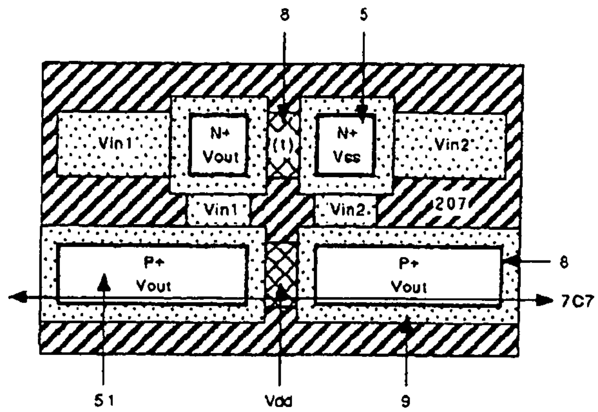


Fig.7C6

Logic circuits (CMOS NAND)



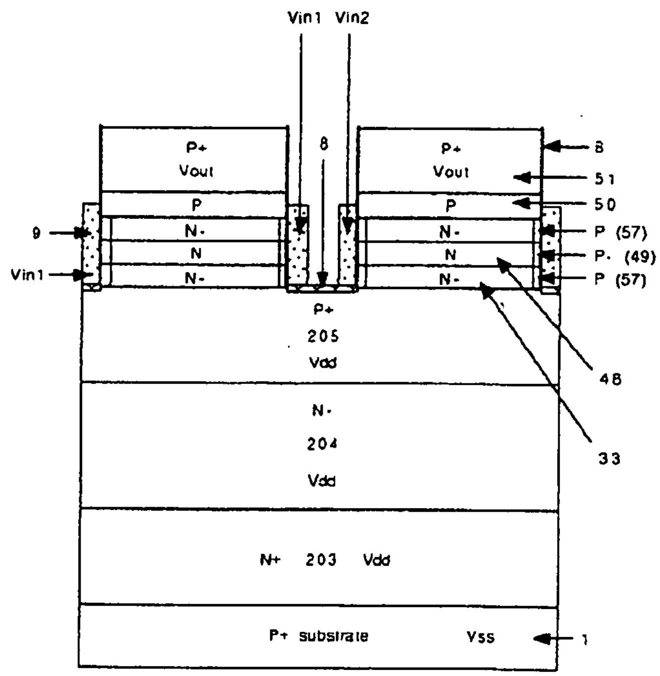


Fig.7C7

Logic circuits (CMOS NAND)

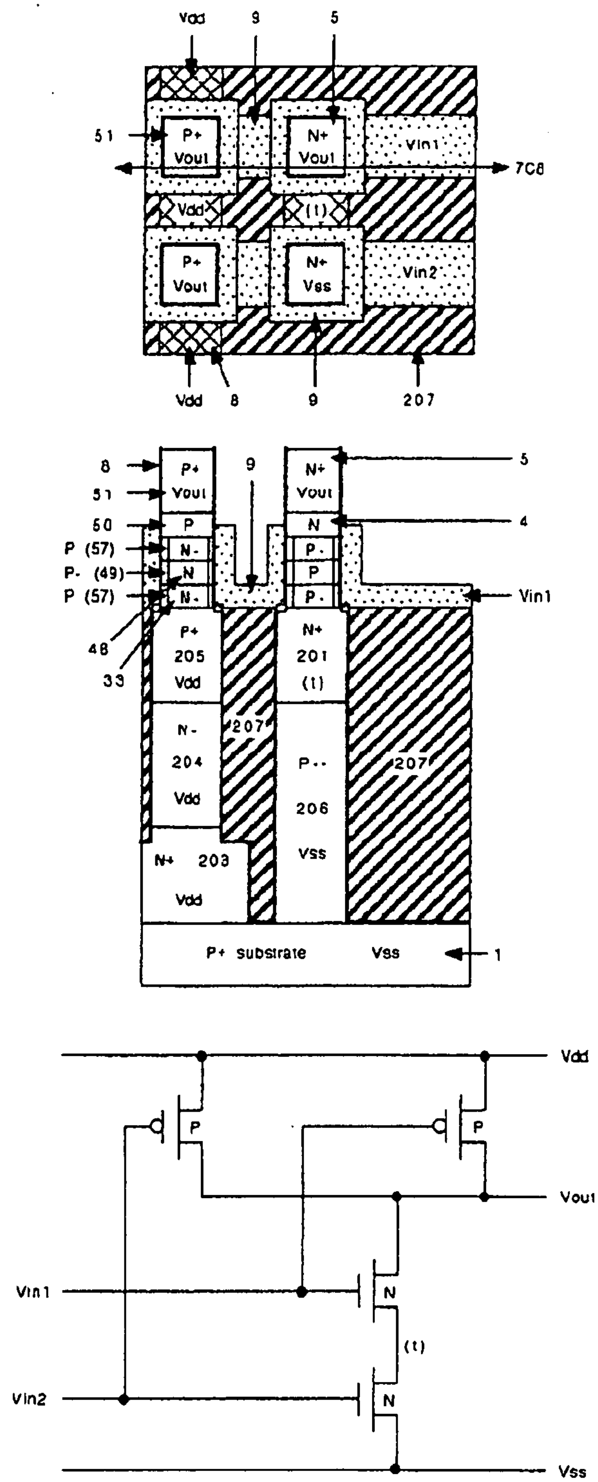


Fig.7C8

Memory Array (SRAM)

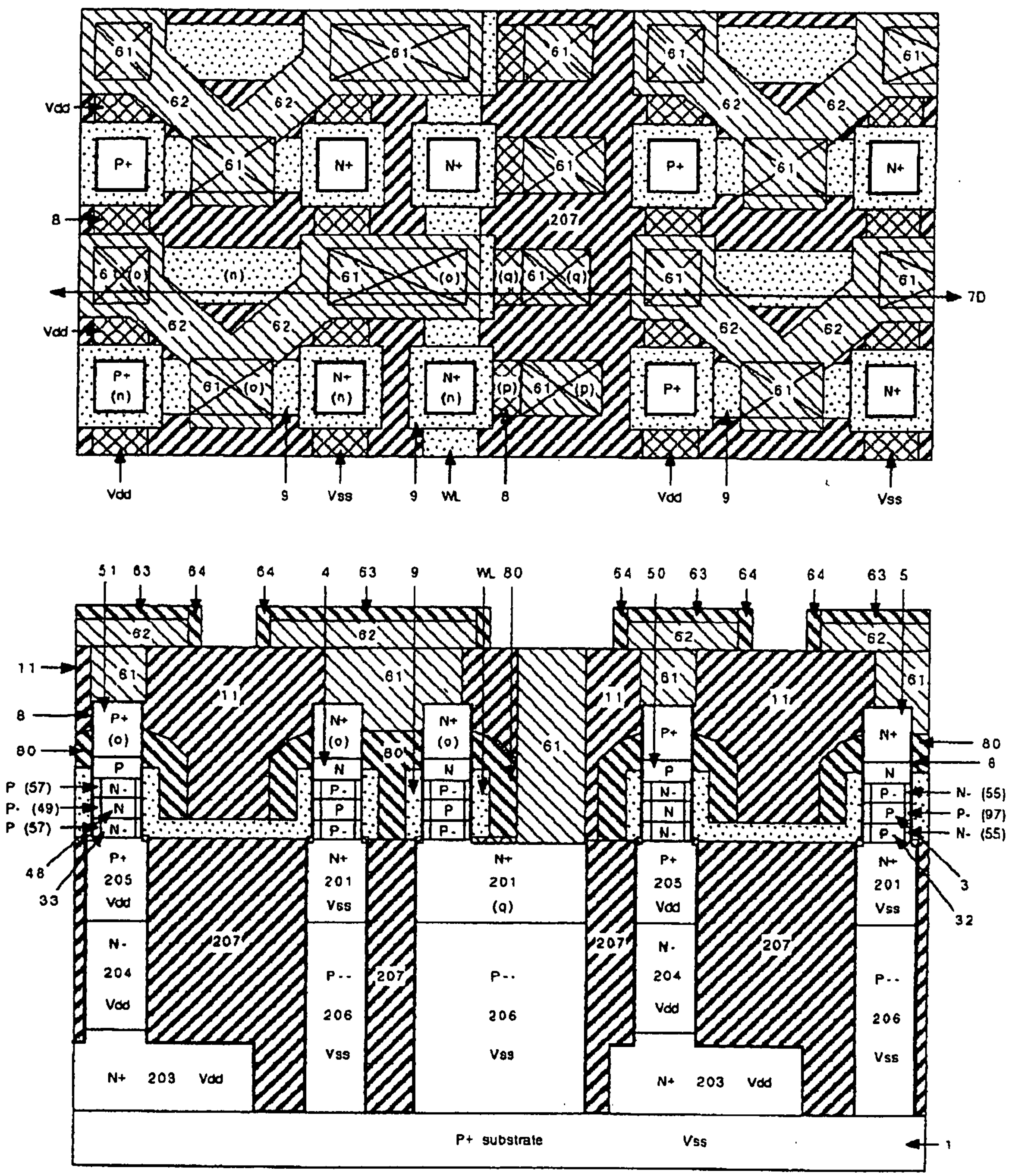
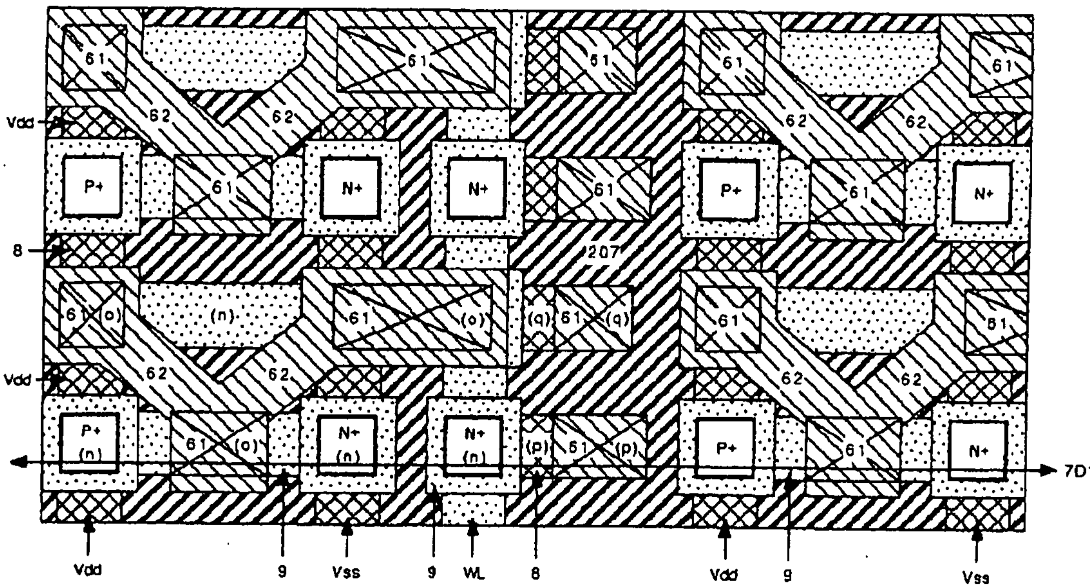


Fig.7D

Memory Array (SRAM)



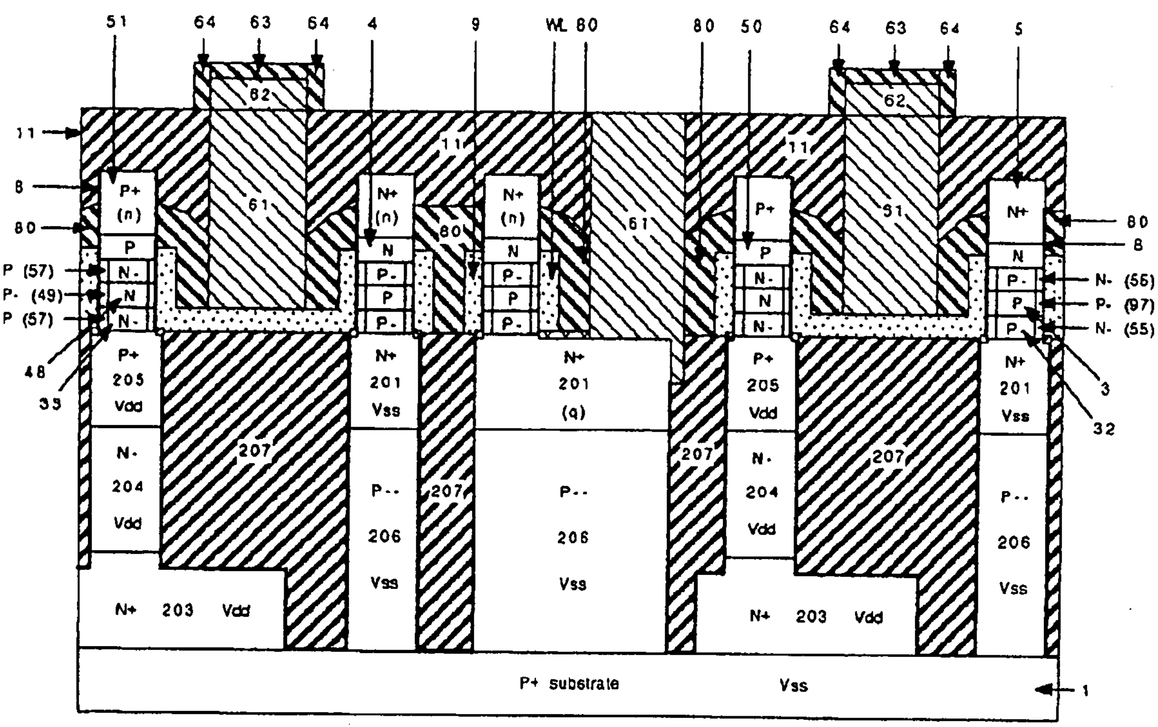


Fig.7D1

Logic Circuits (A Full Adder)

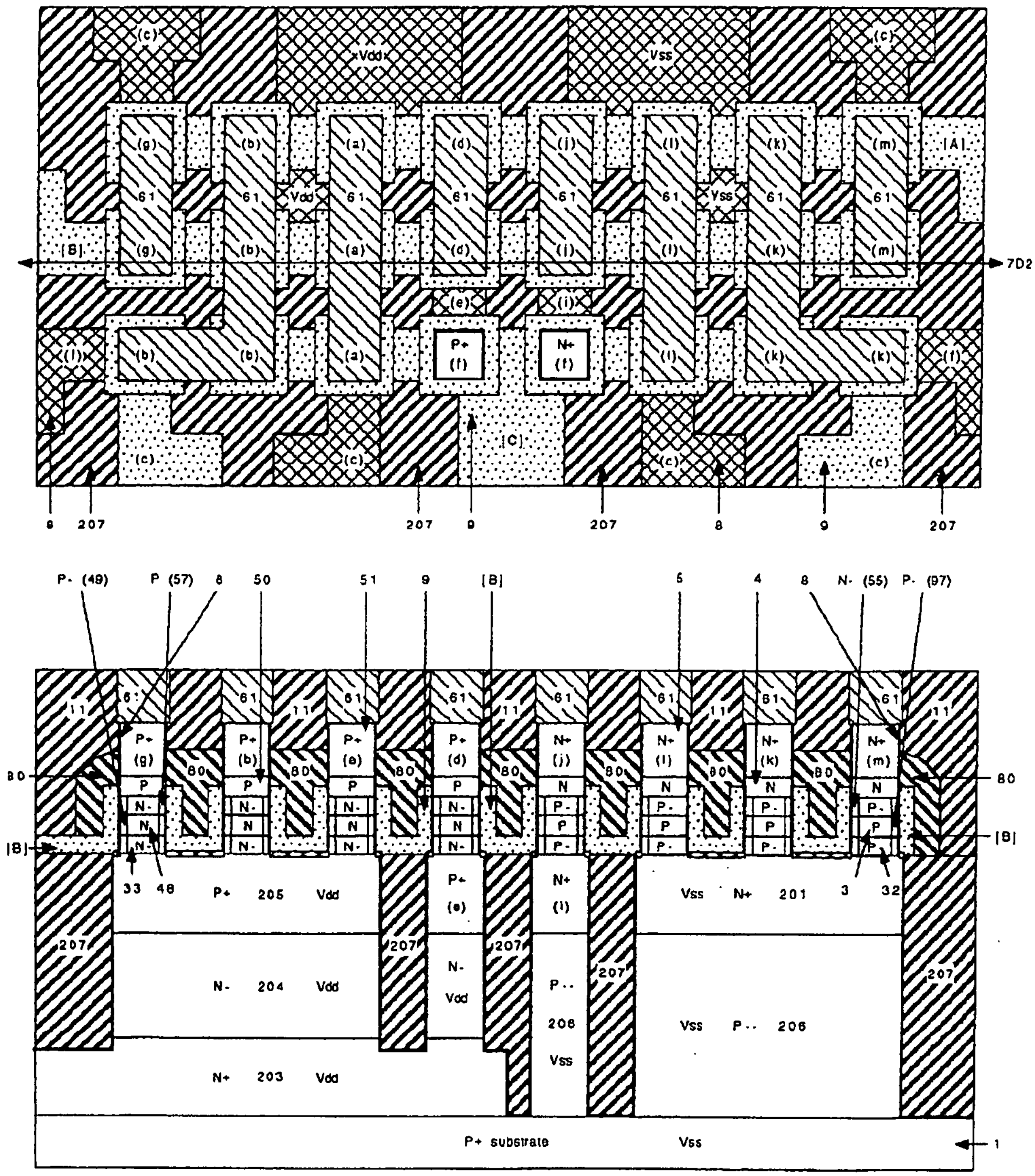


Fig.7D2

Logic Circuits (A Full Adder)

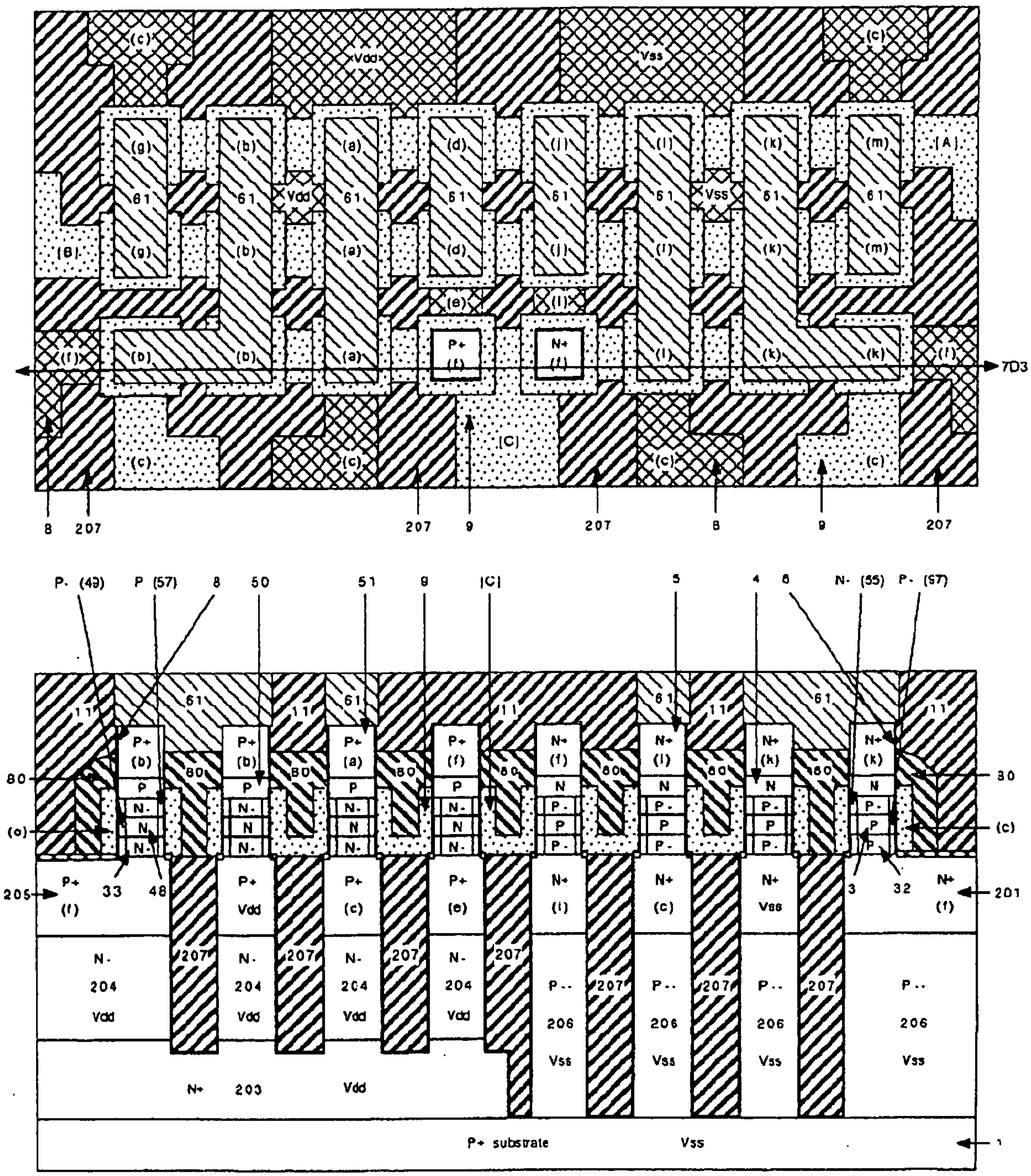
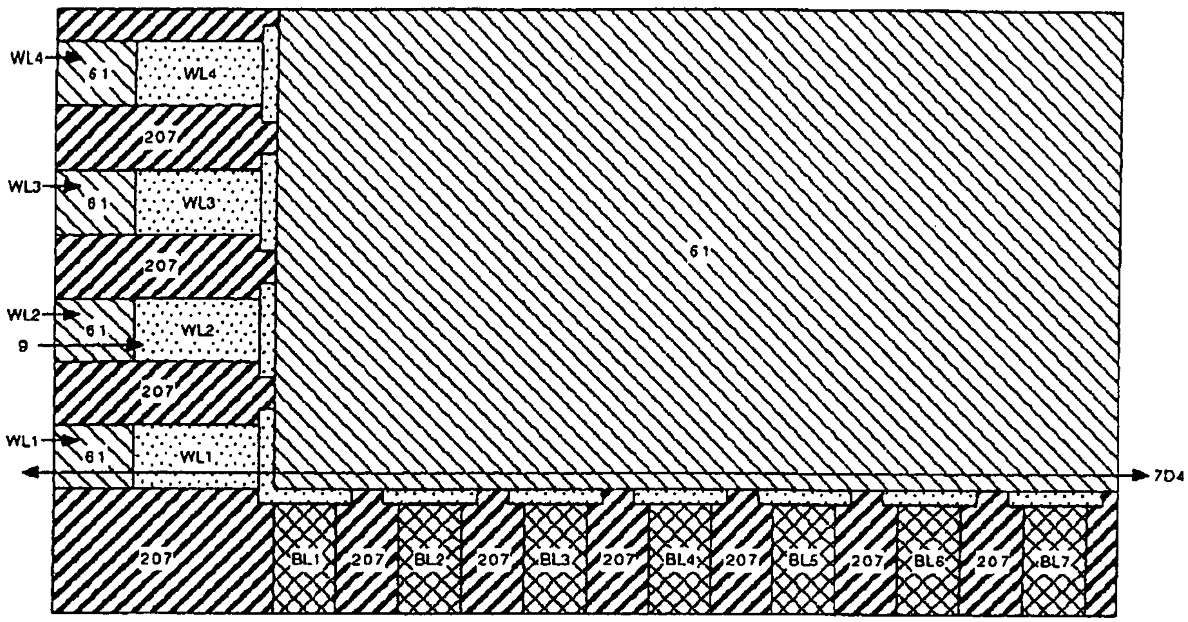


Fig.7D3

Memory Array (DRAM)



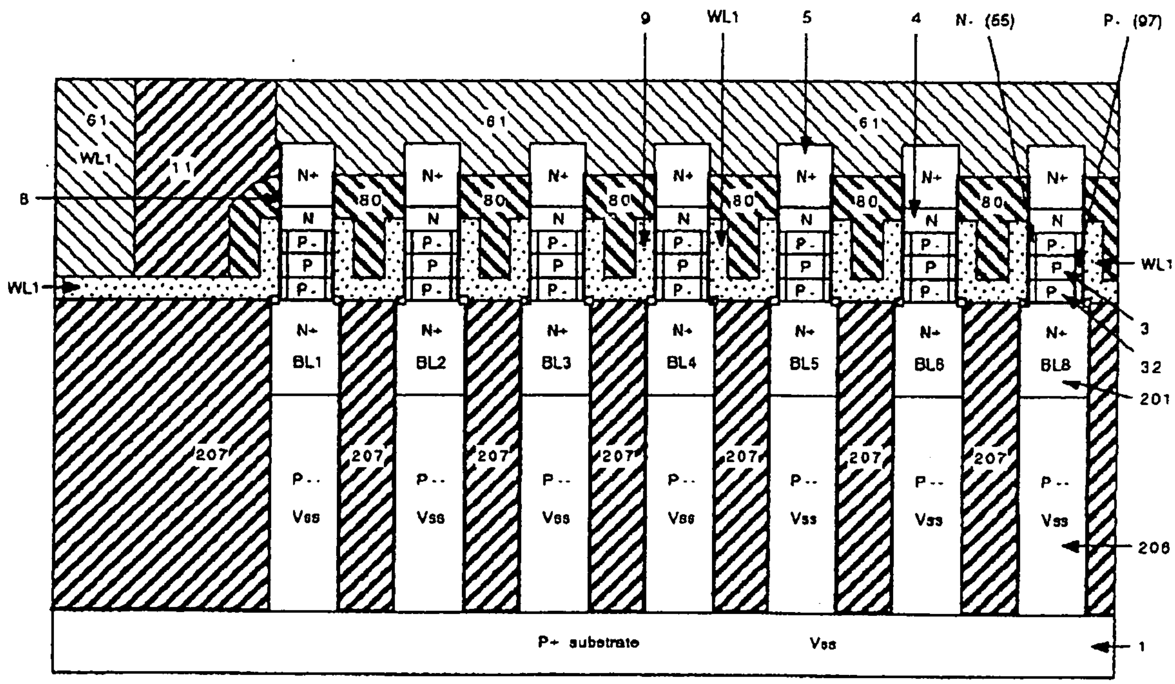
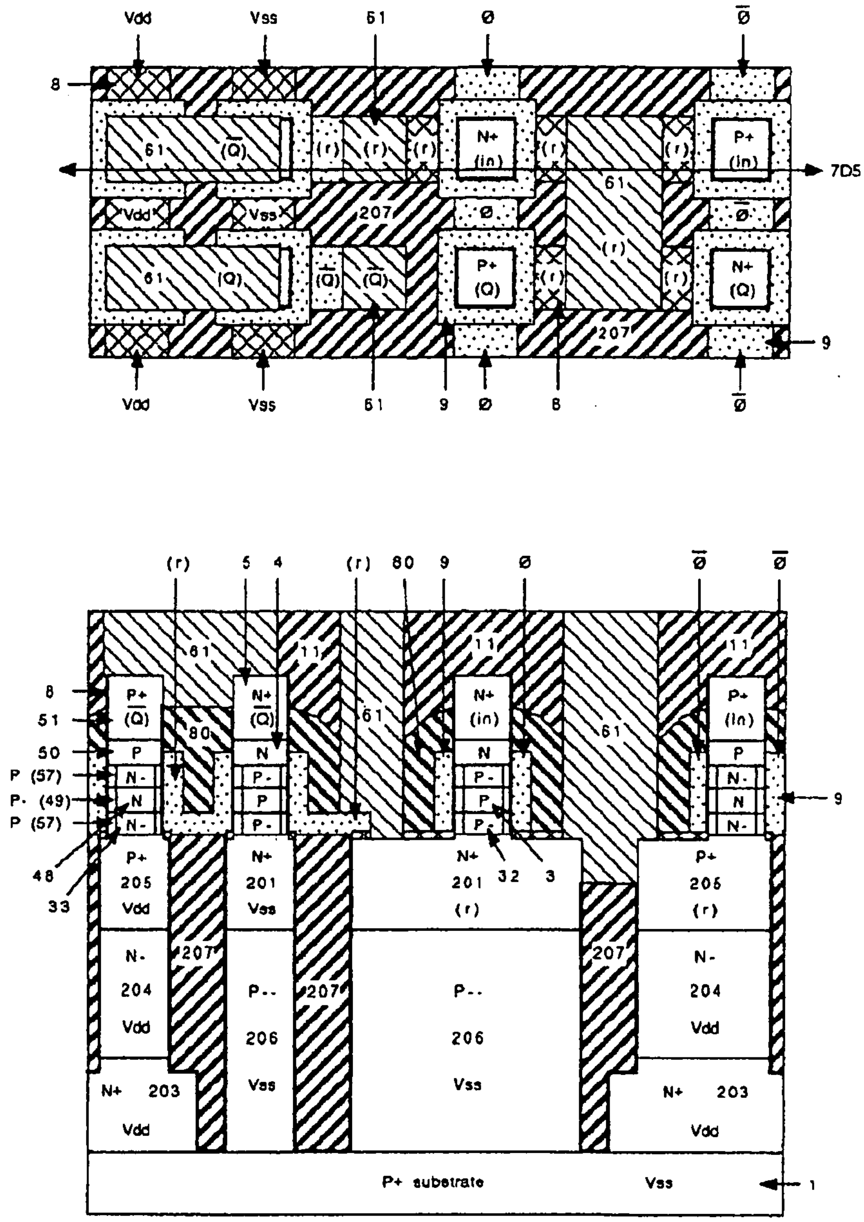
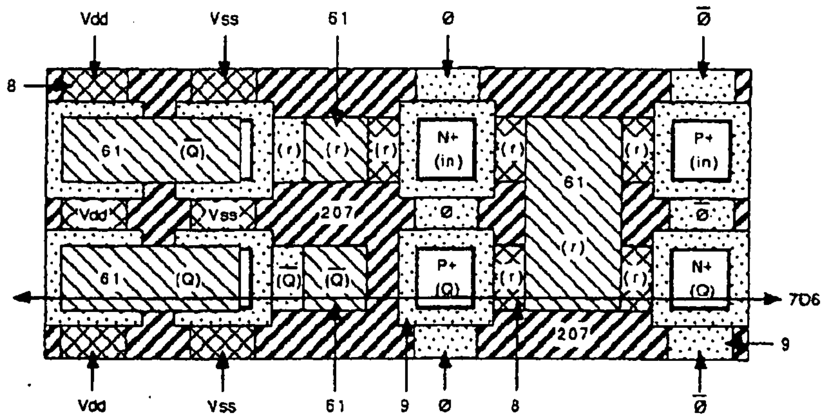


Fig.7D4

Logic circuits (CMOS flip-flop)



Logic circuits (CMOS flip-flop)



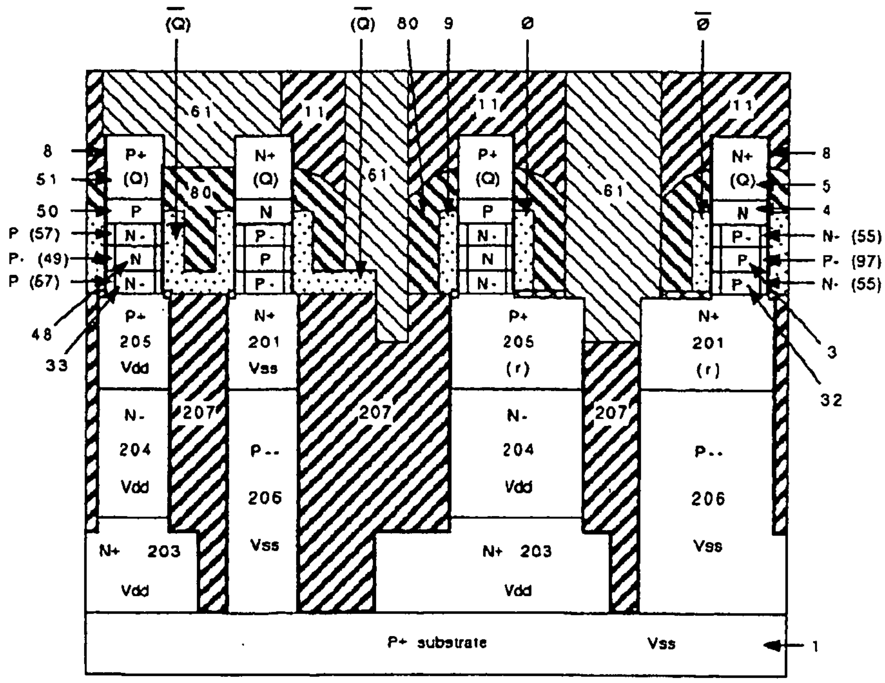
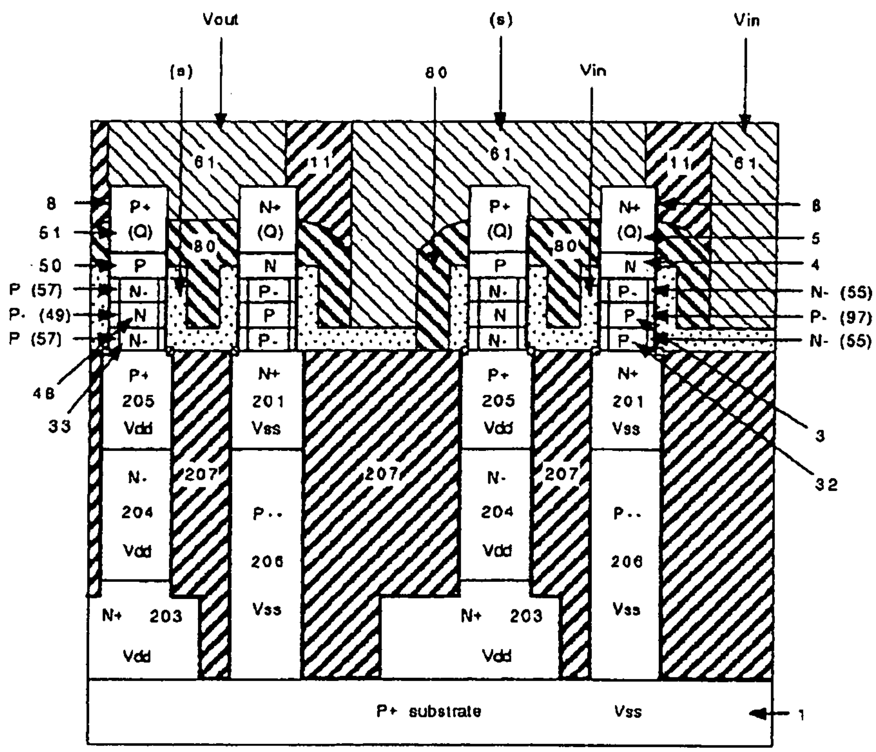


Fig.7D6

Logic circuits (CMOS inverter chain)



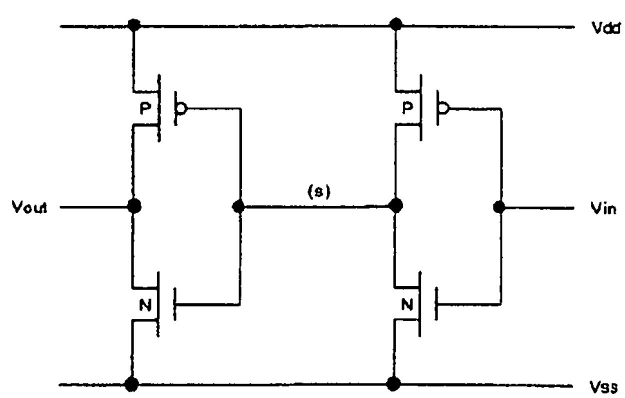
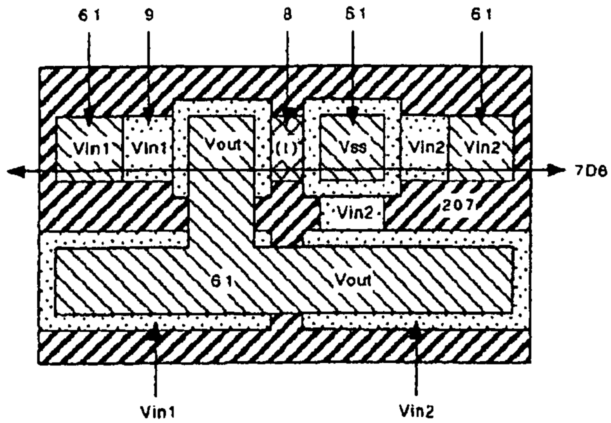


Fig.7D7

Logic circuits (CMOS NAND)



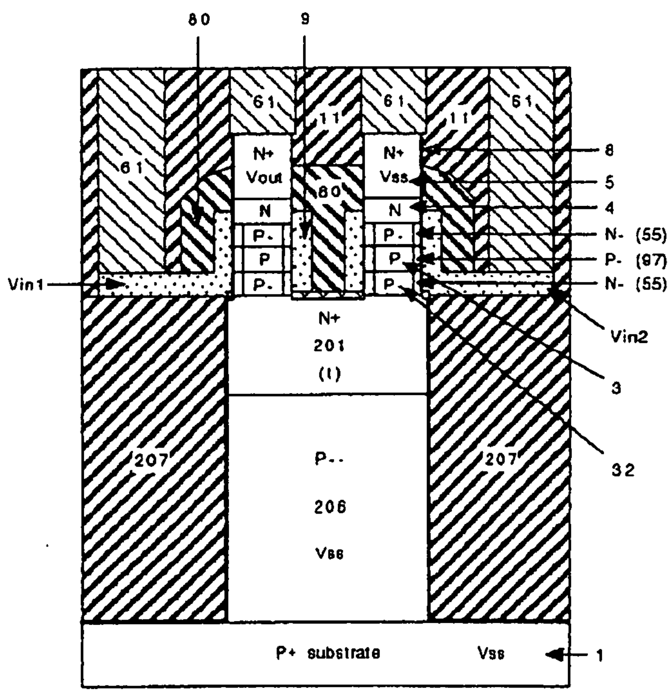
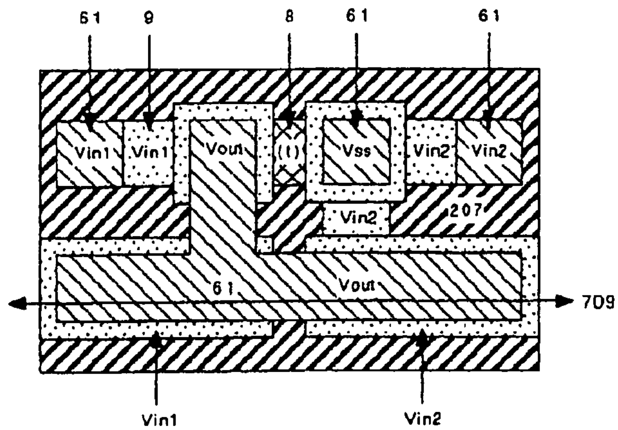


Fig.7D8

Logic circuits (CMOS NAND)



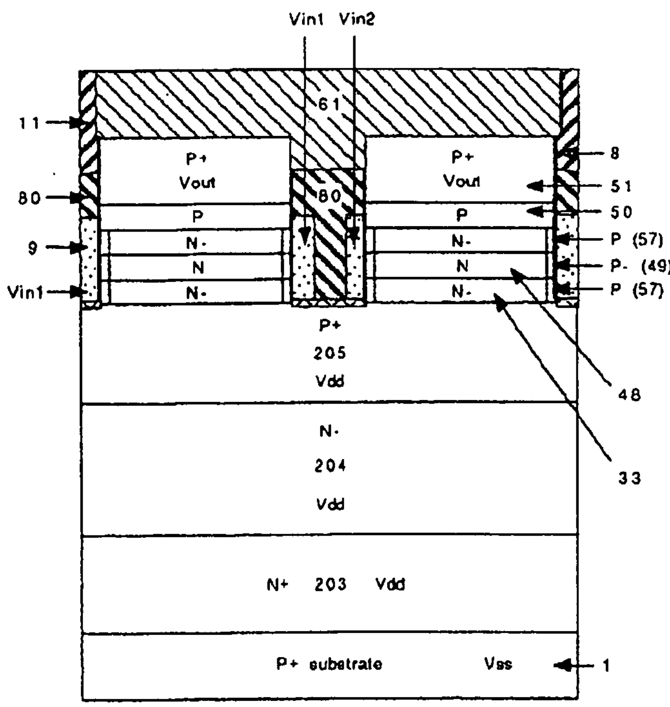
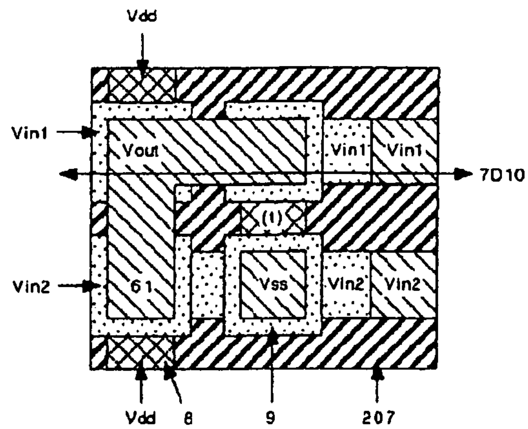


Fig.7D9

Logic circuits (CMOS NAND)



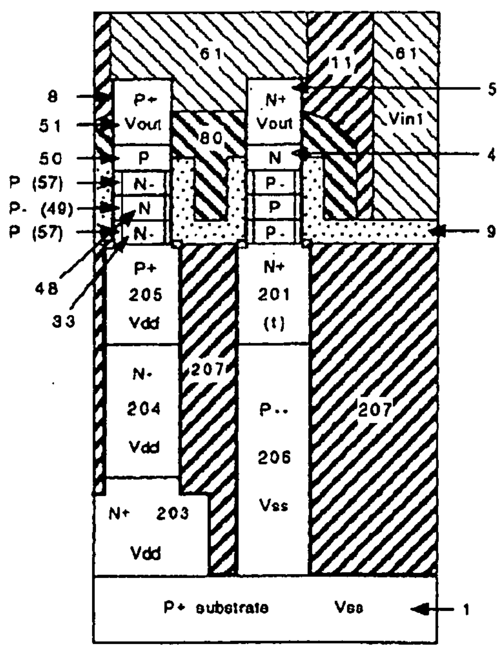
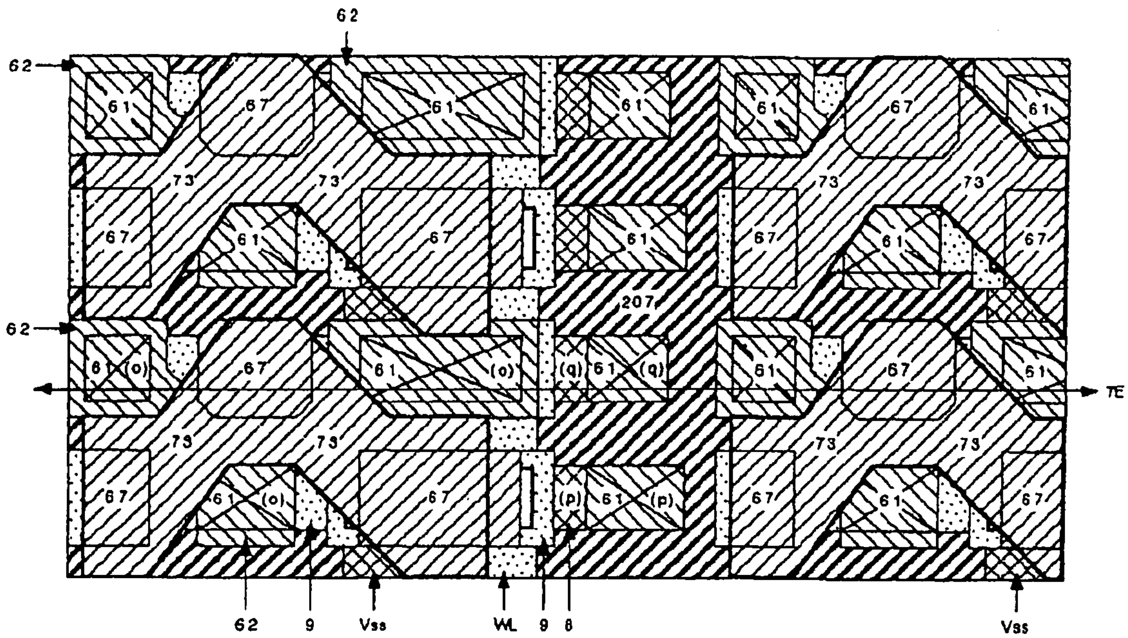


Fig.7D10

Memory Array (SRAM)



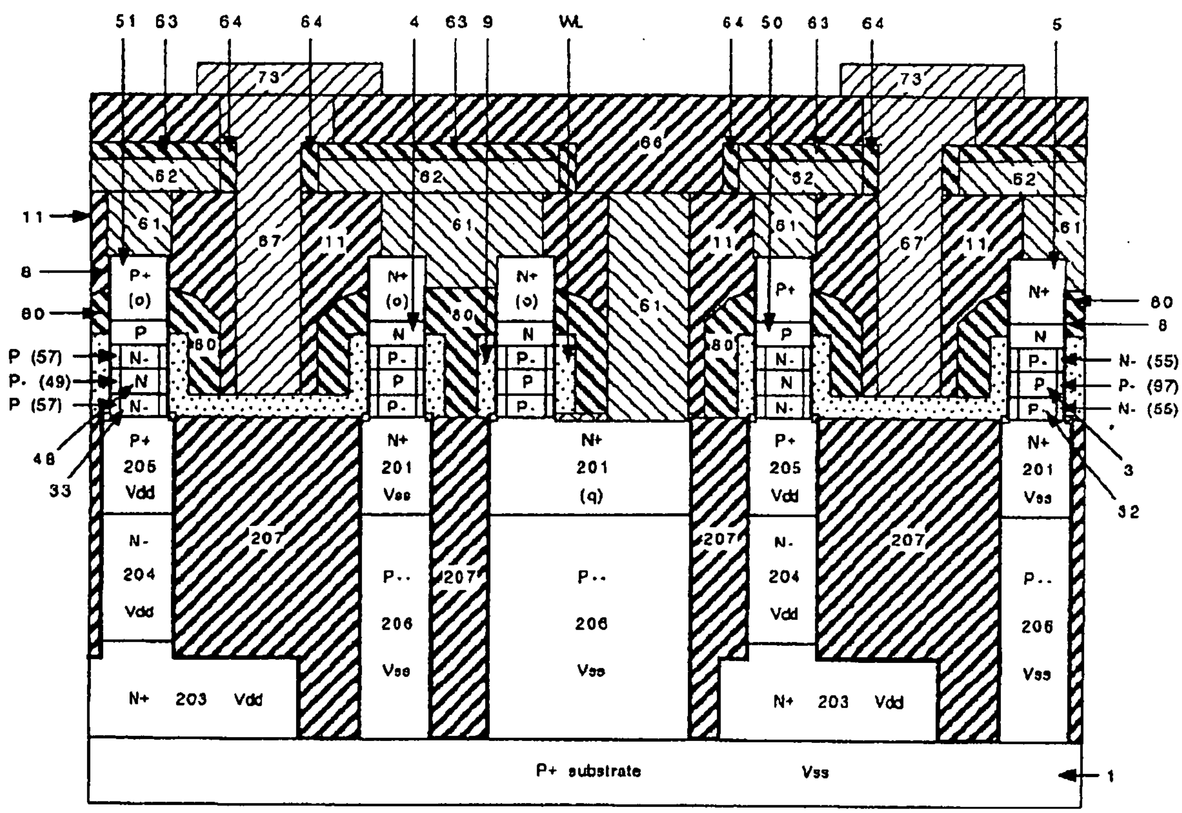


Fig.7E

Memory Array (SRAM)

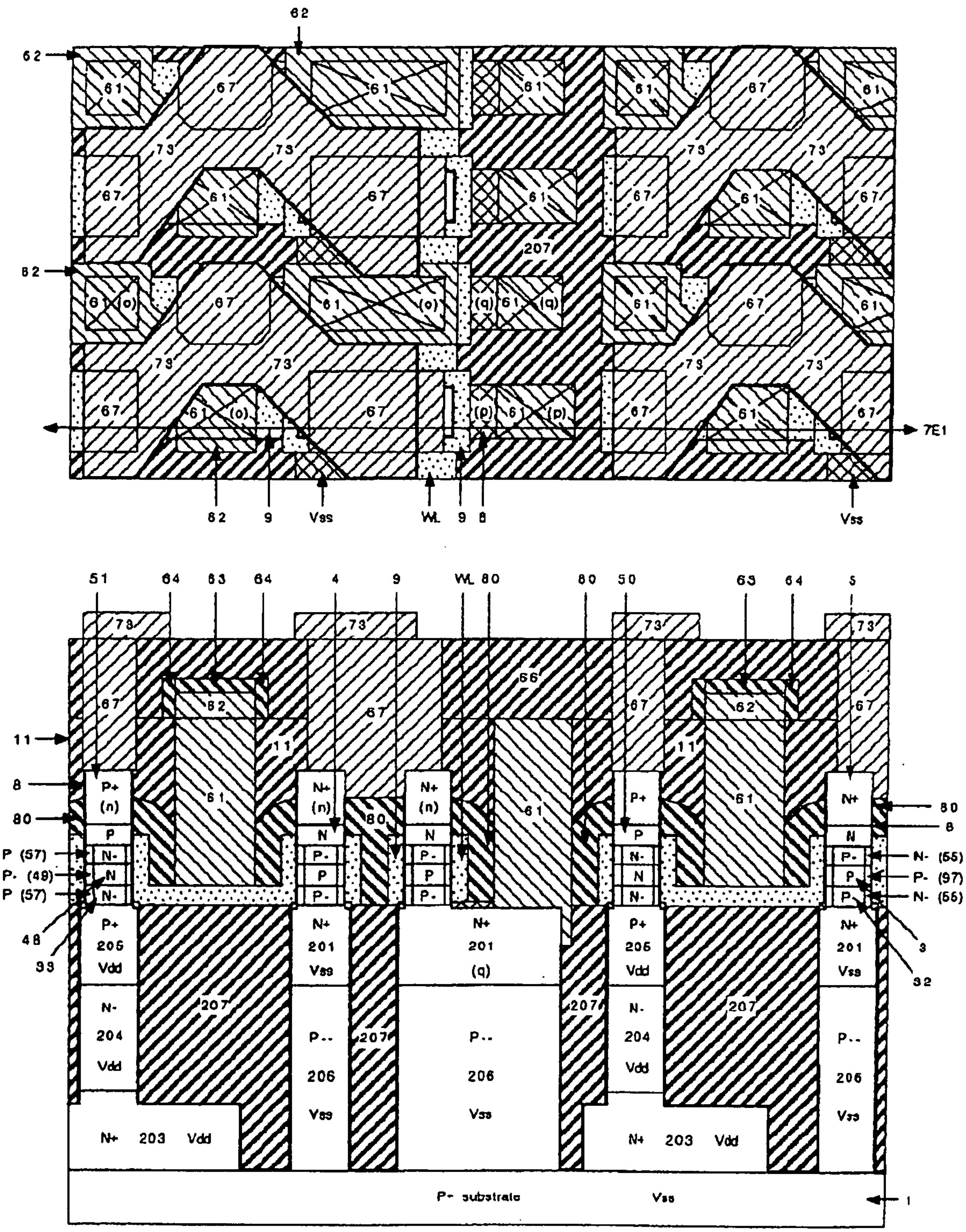


Fig.7E1

Logic Circuits (A Full Adder)

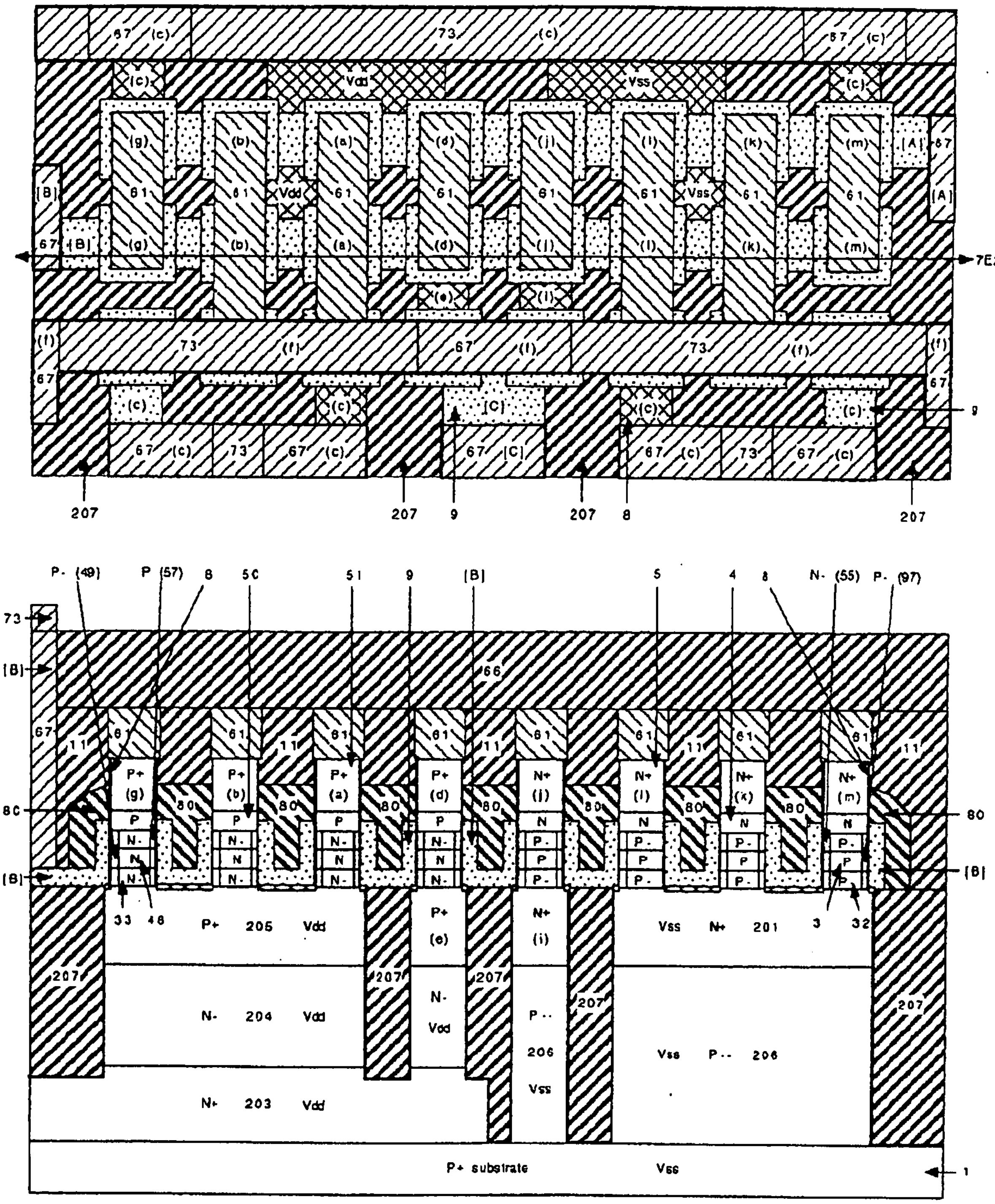


Fig.7E2

Logic Circuits (A Full Adder)

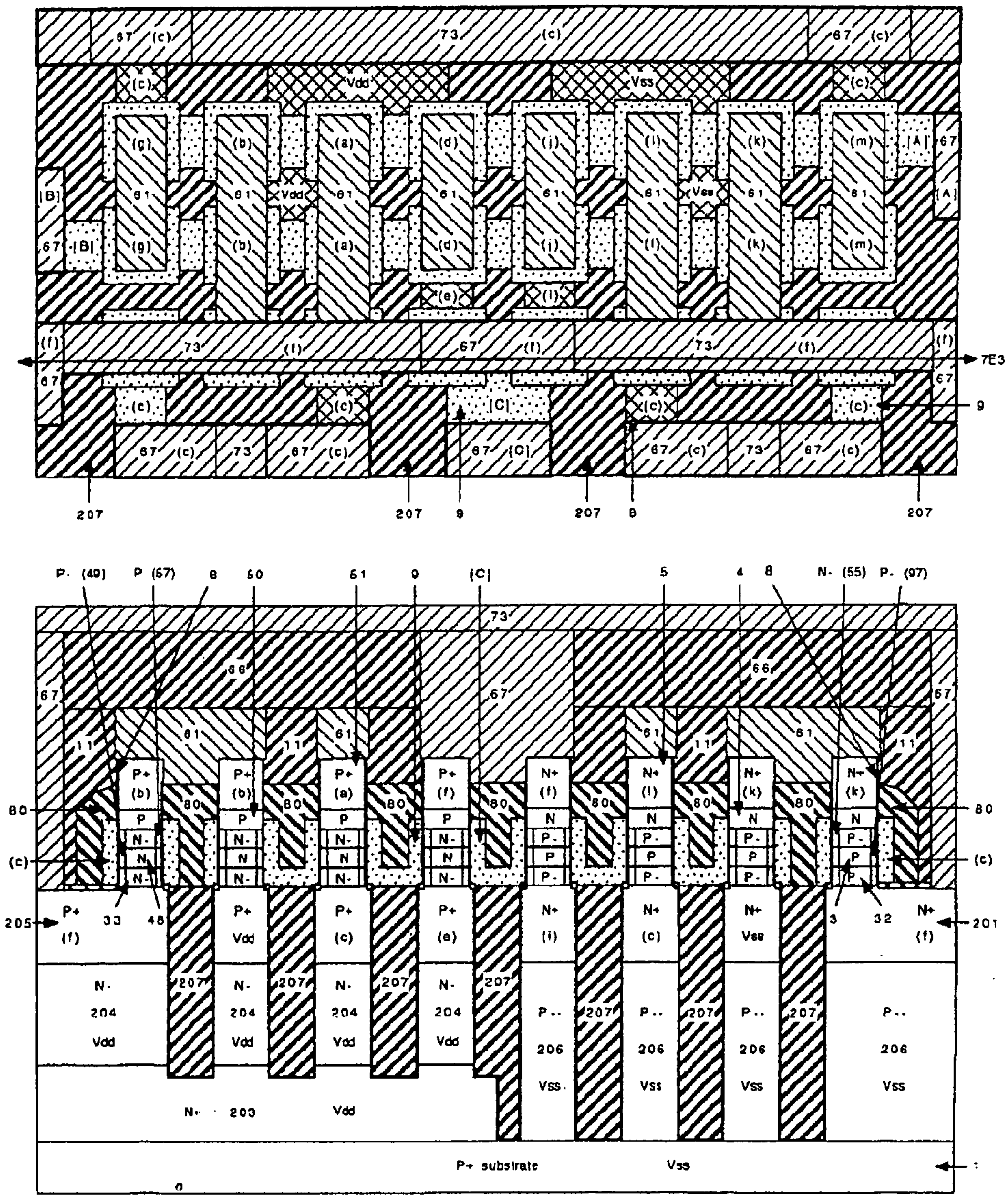


Fig.7E3

Logic circuits (CMOS flip-flop)

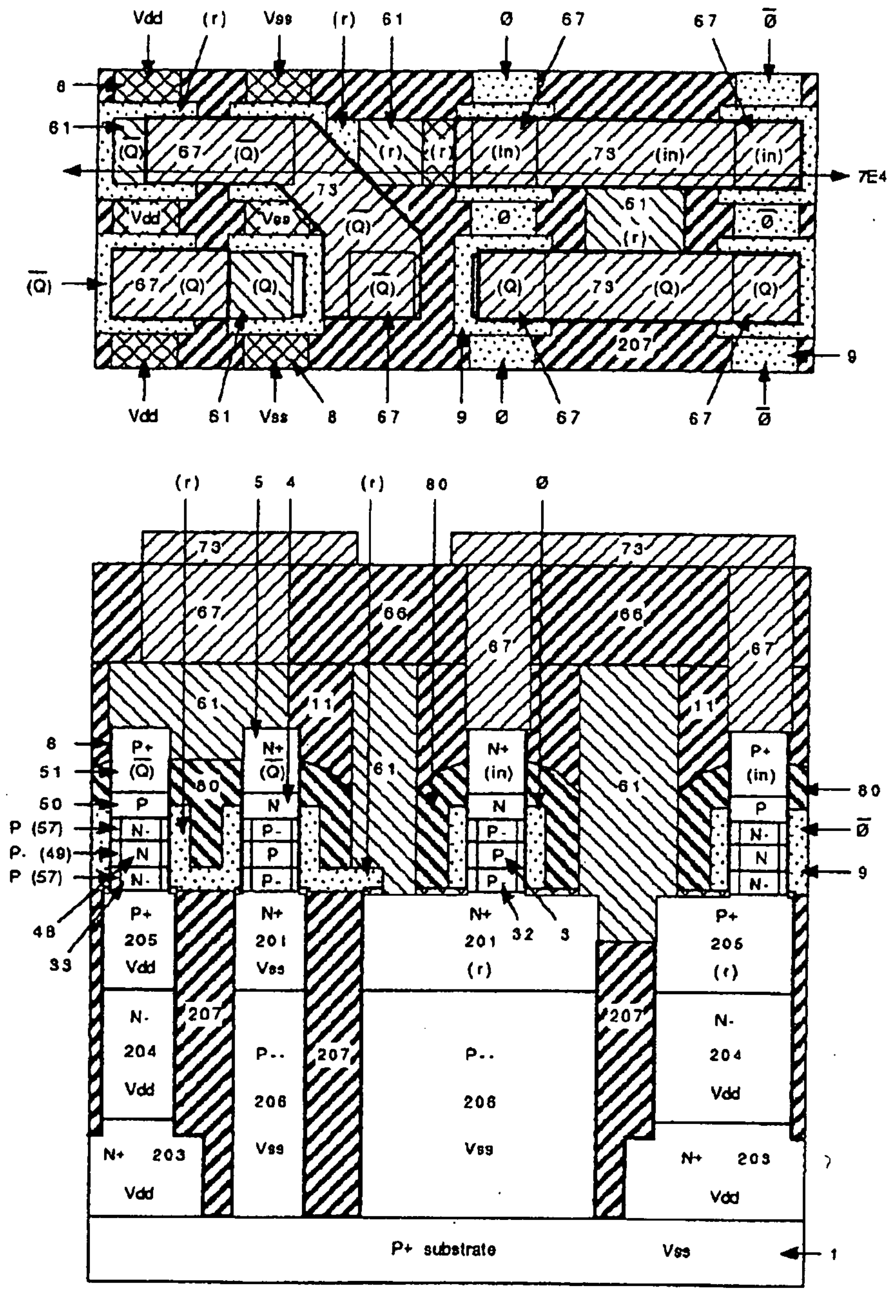


Fig.7E4

Logic circuits (CMOS flip-flop)

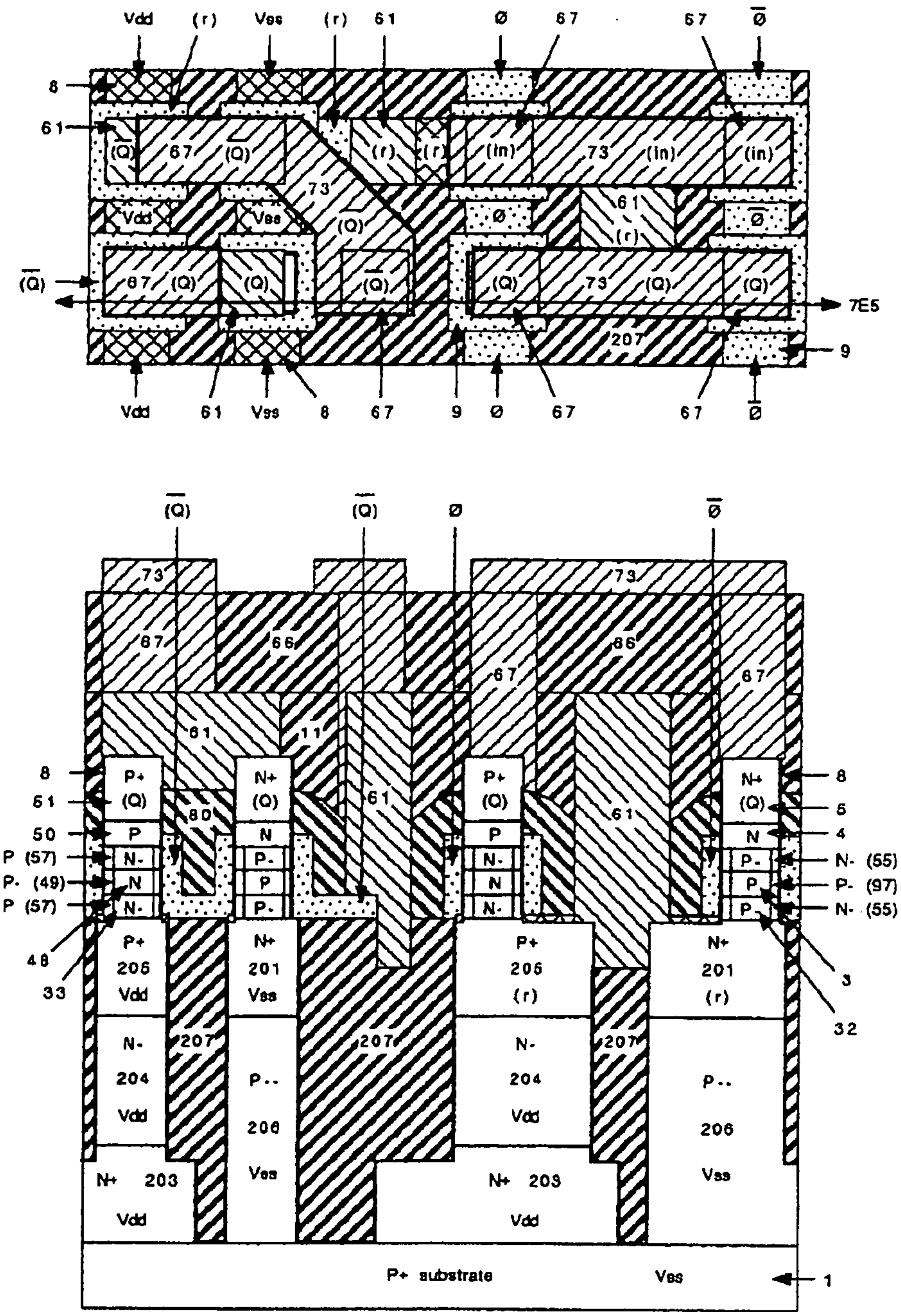


Fig.7E5

Logic circuits (CMOS NAND)

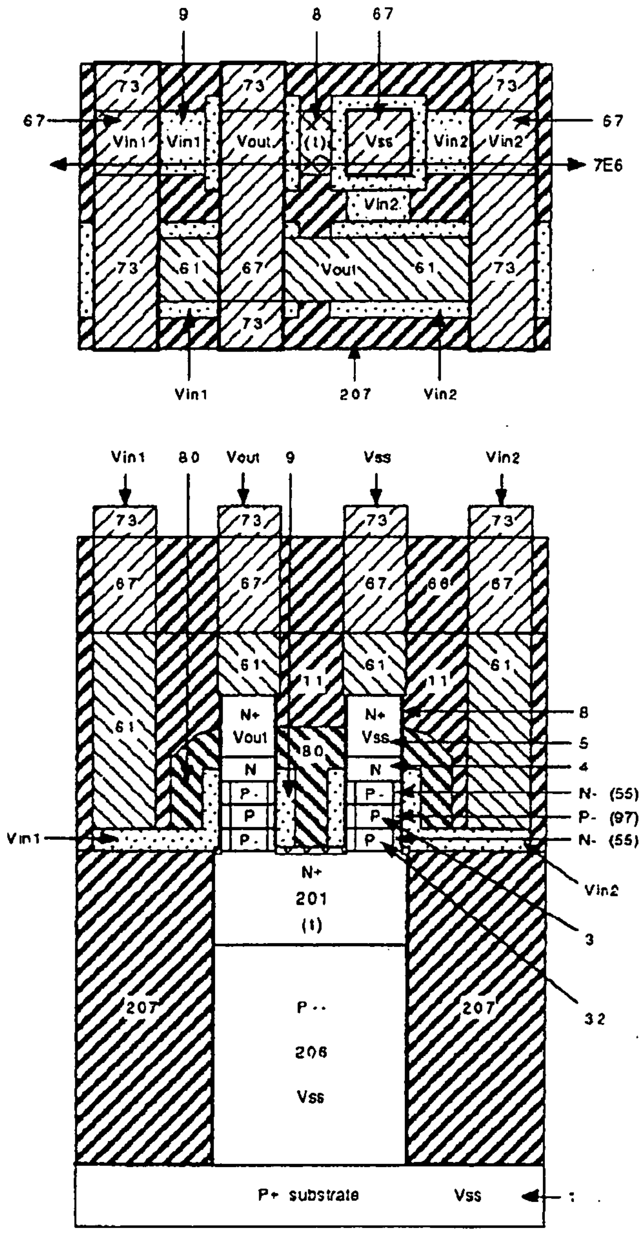
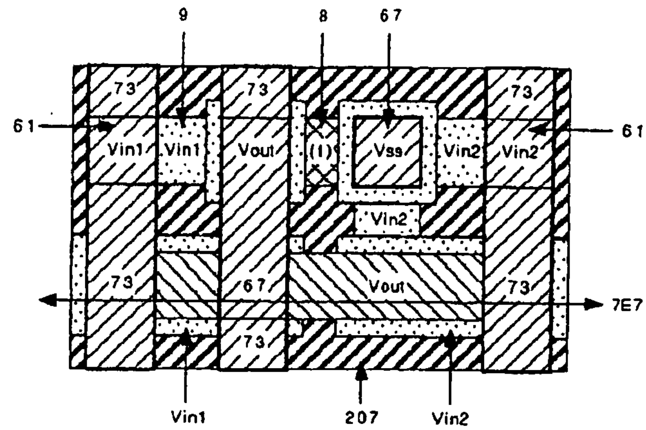


Fig.7E6

Logic circuits (CMOS NAND)



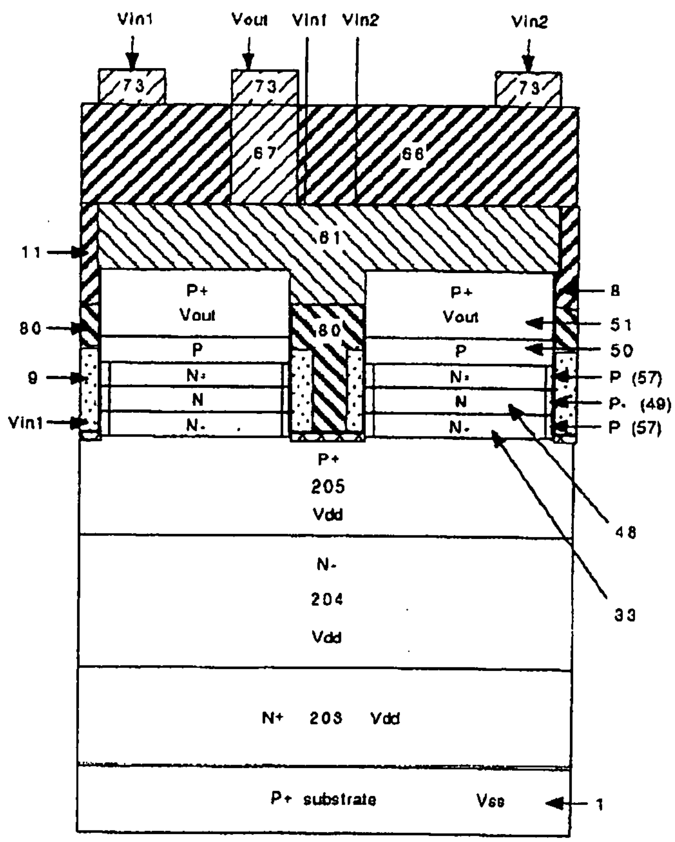


Fig.7E7

Logic circuits (CMOS NAND)

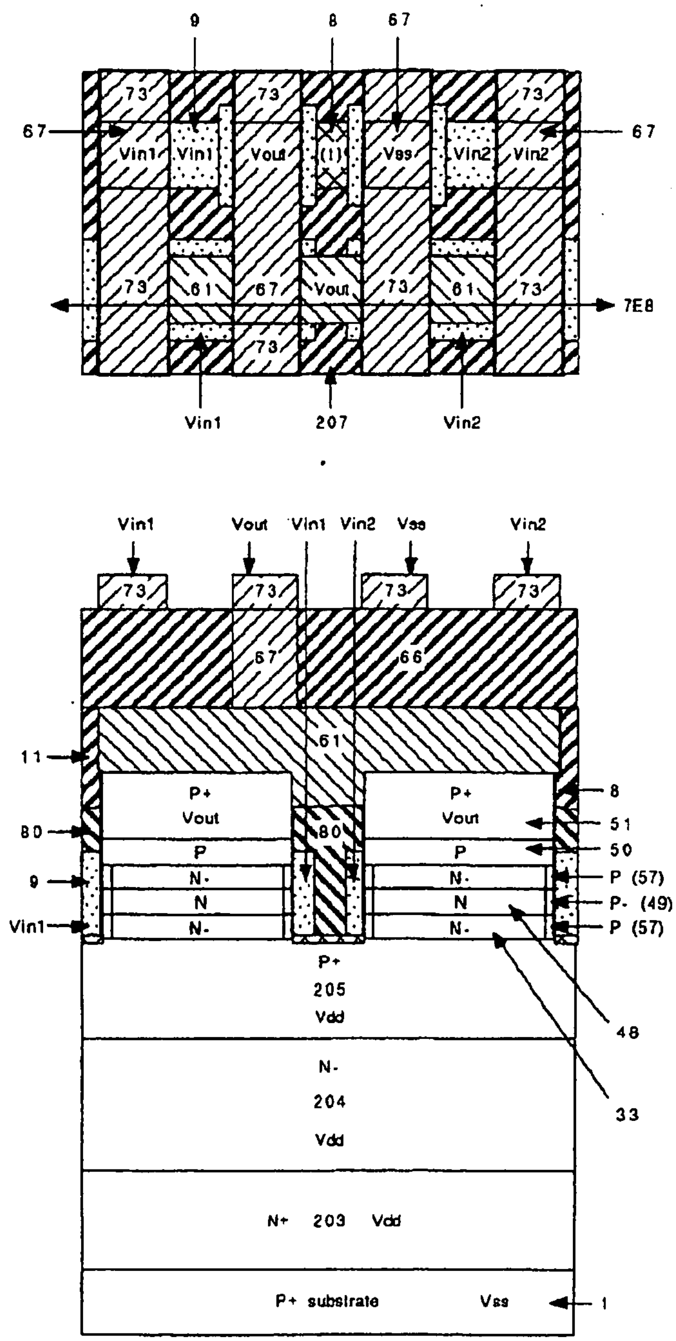


Fig.7E8

Logic circuits (CMOS NAND)

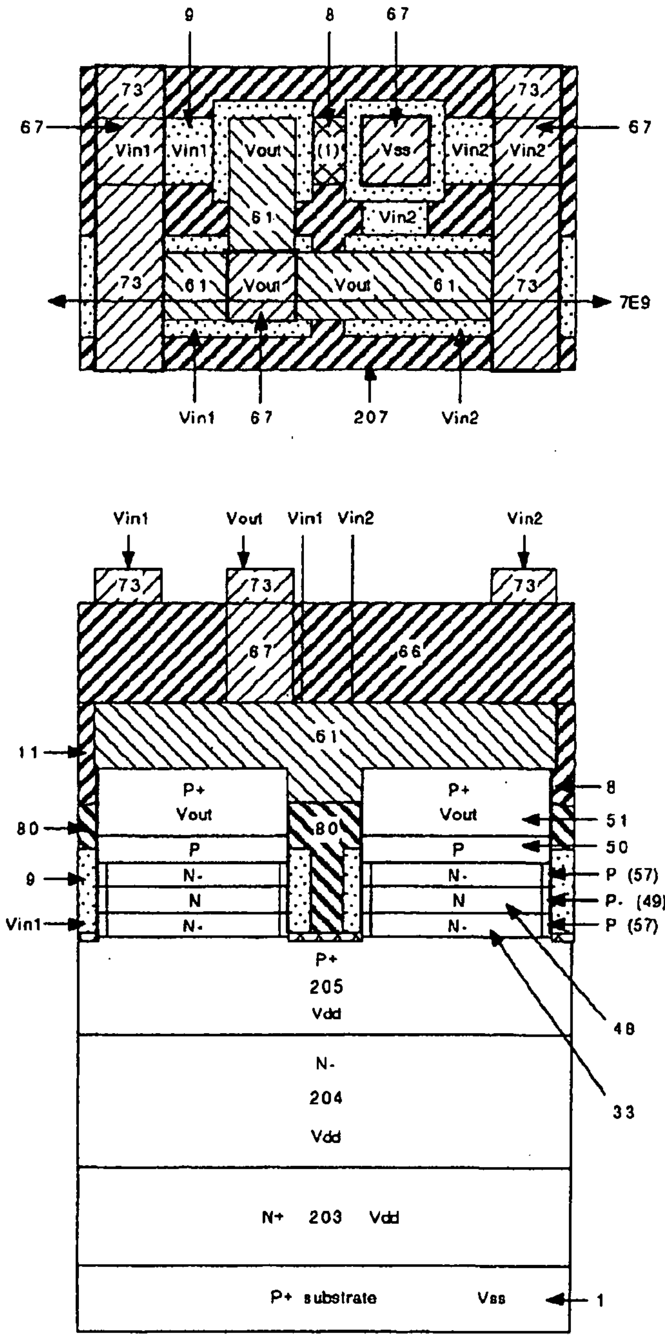
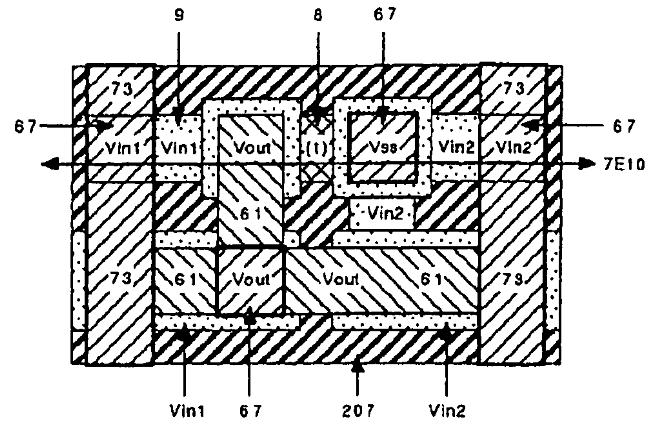


Fig.7E9

Logic circuits (CMOS NAND)



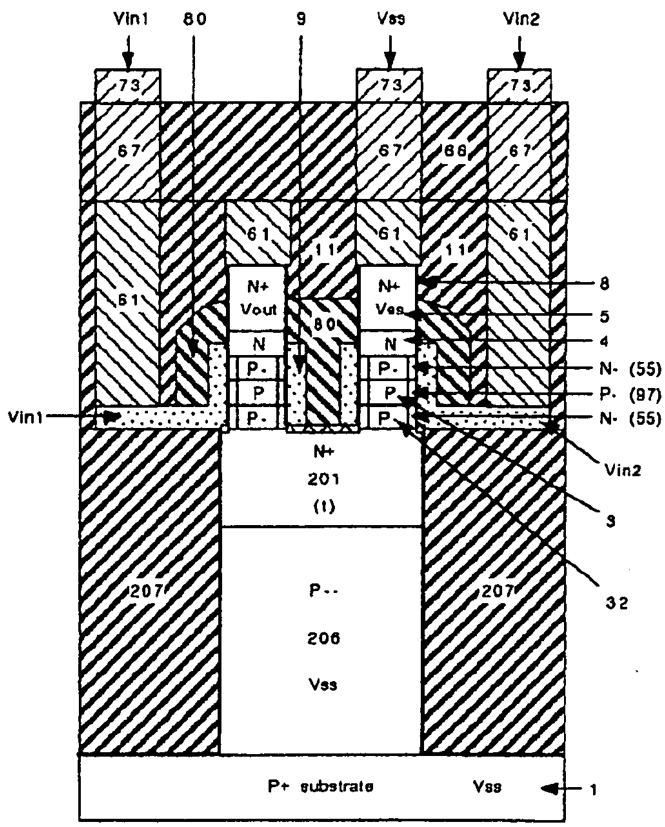


Fig.7E10

Logic circuits (CMOS NAND)

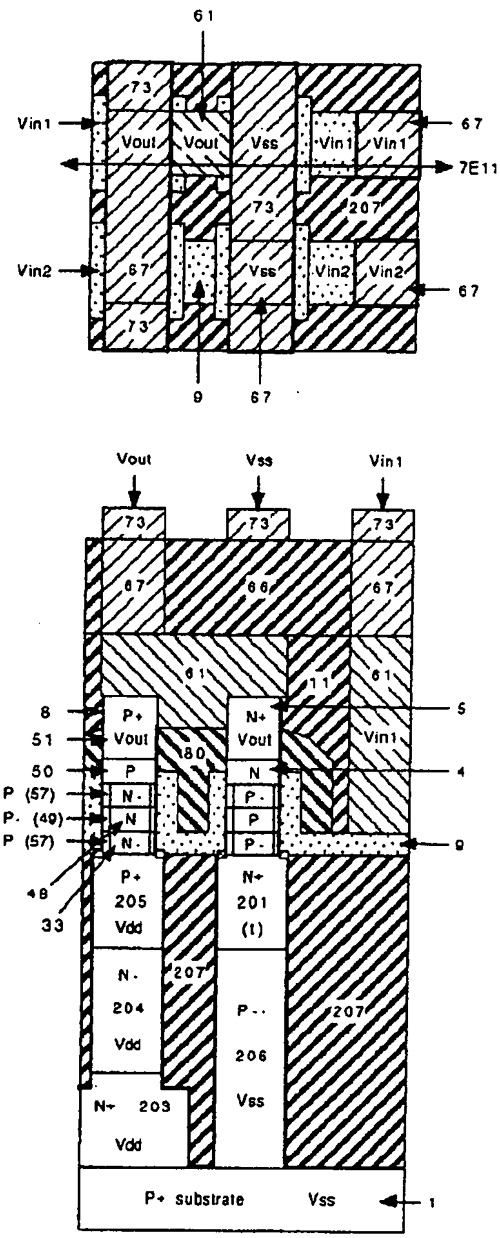


Fig.7E11

Memory Array (DRAM)

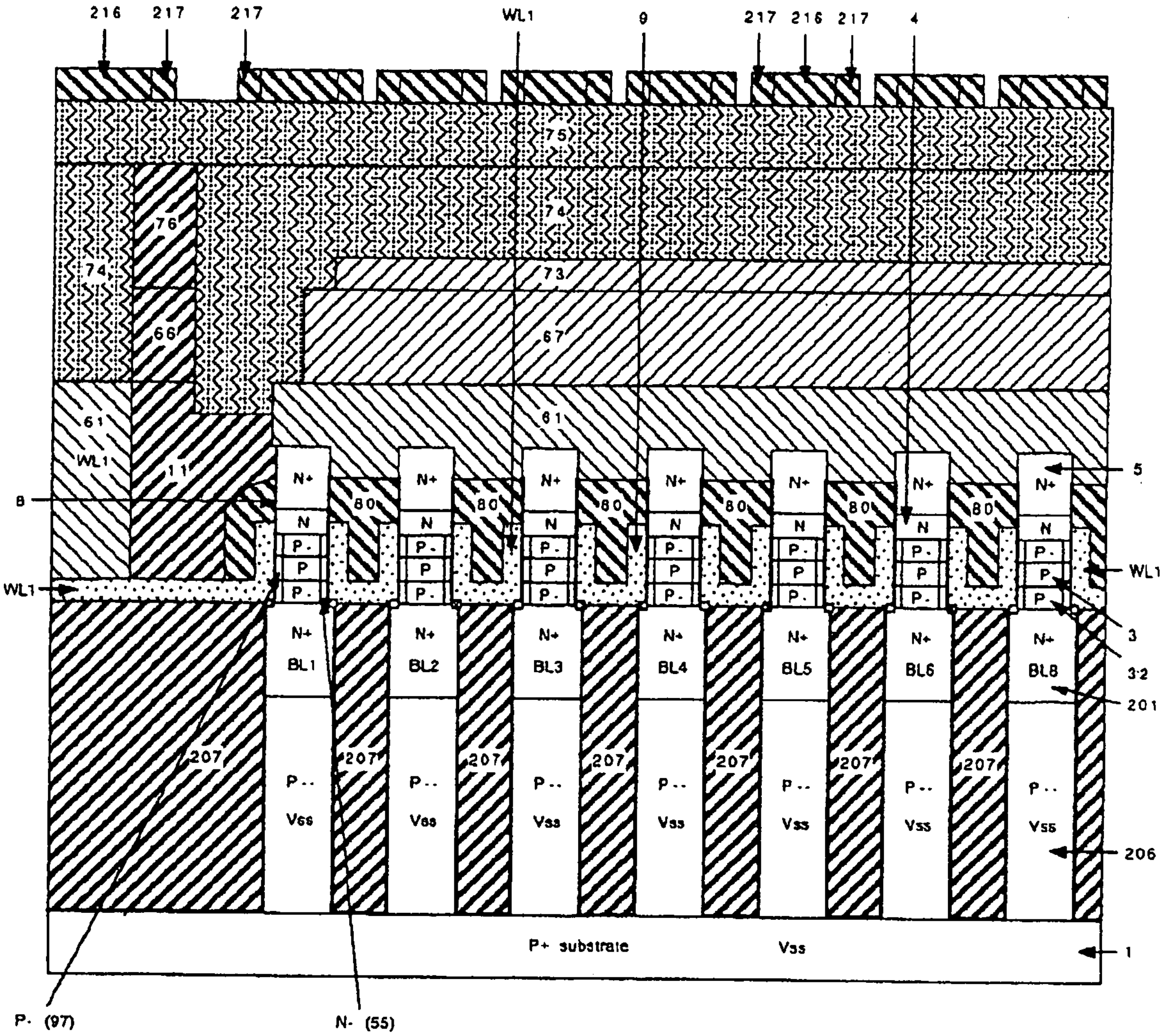


Fig.7F

Memory Array (DRAM)

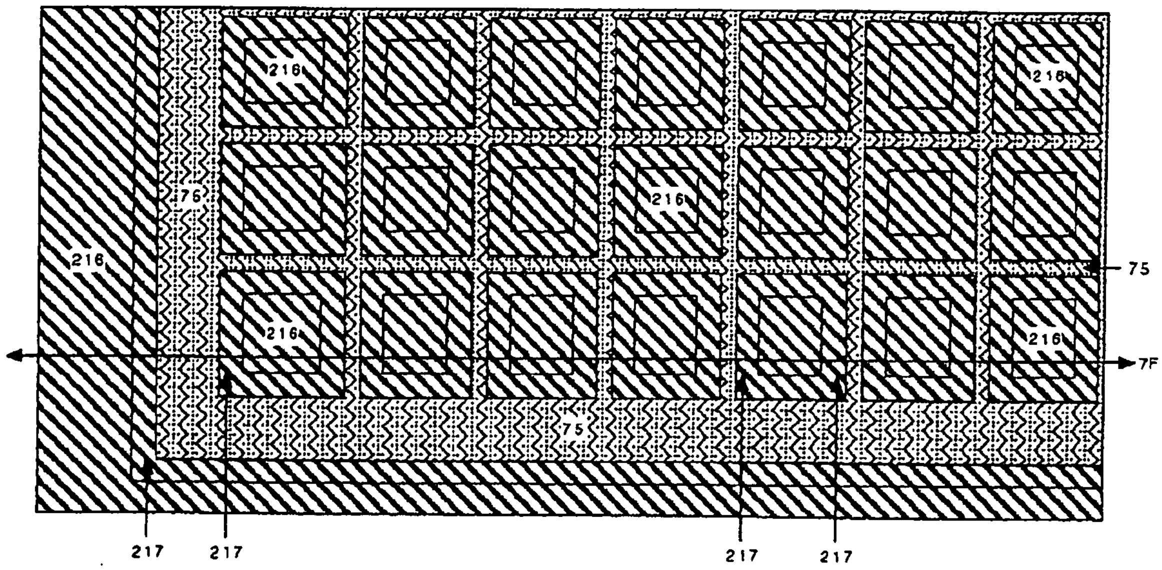


Fig.7F1

Memory Array (DRAM)

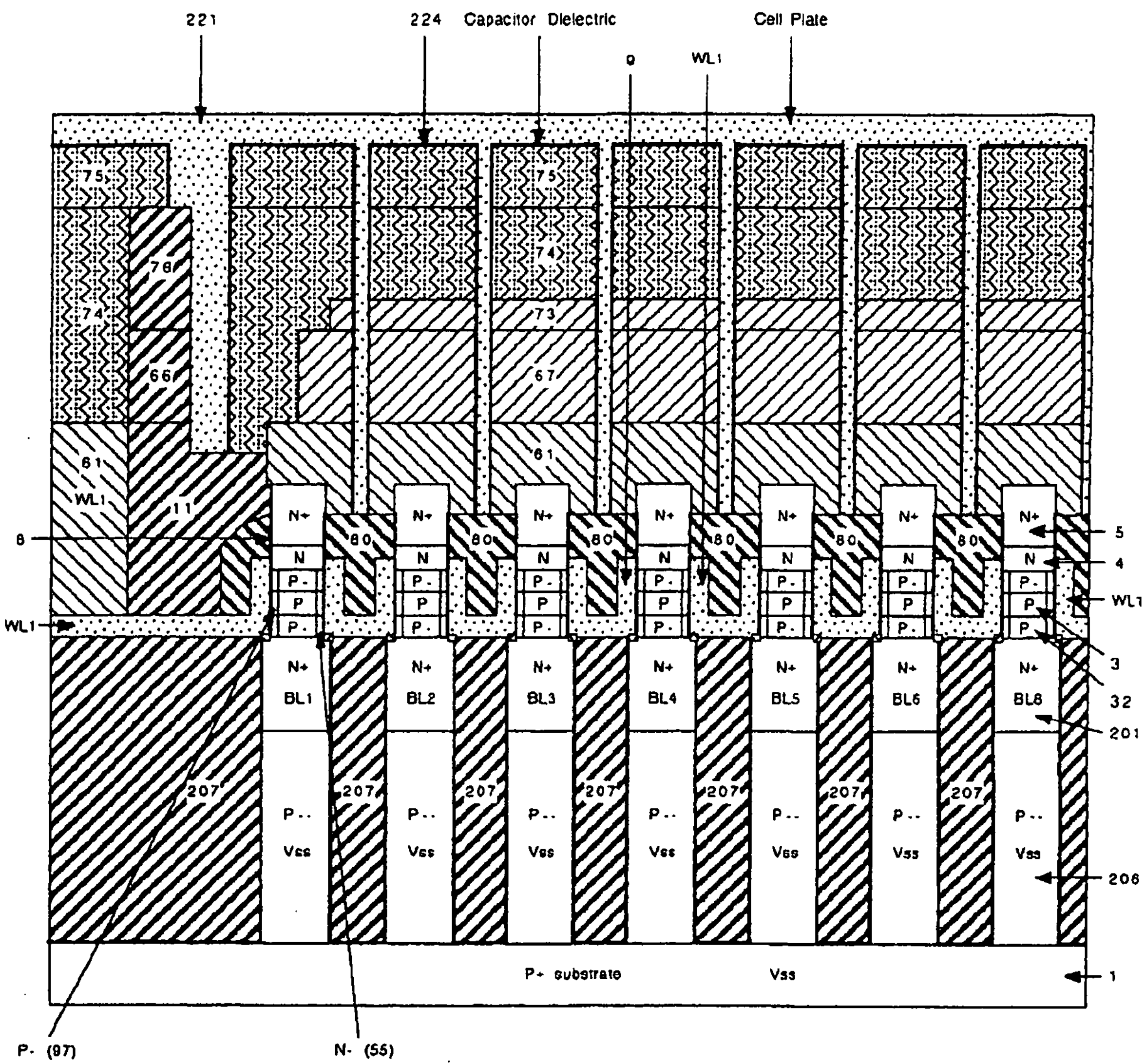


Fig.7G

Memory Array (DRAM)

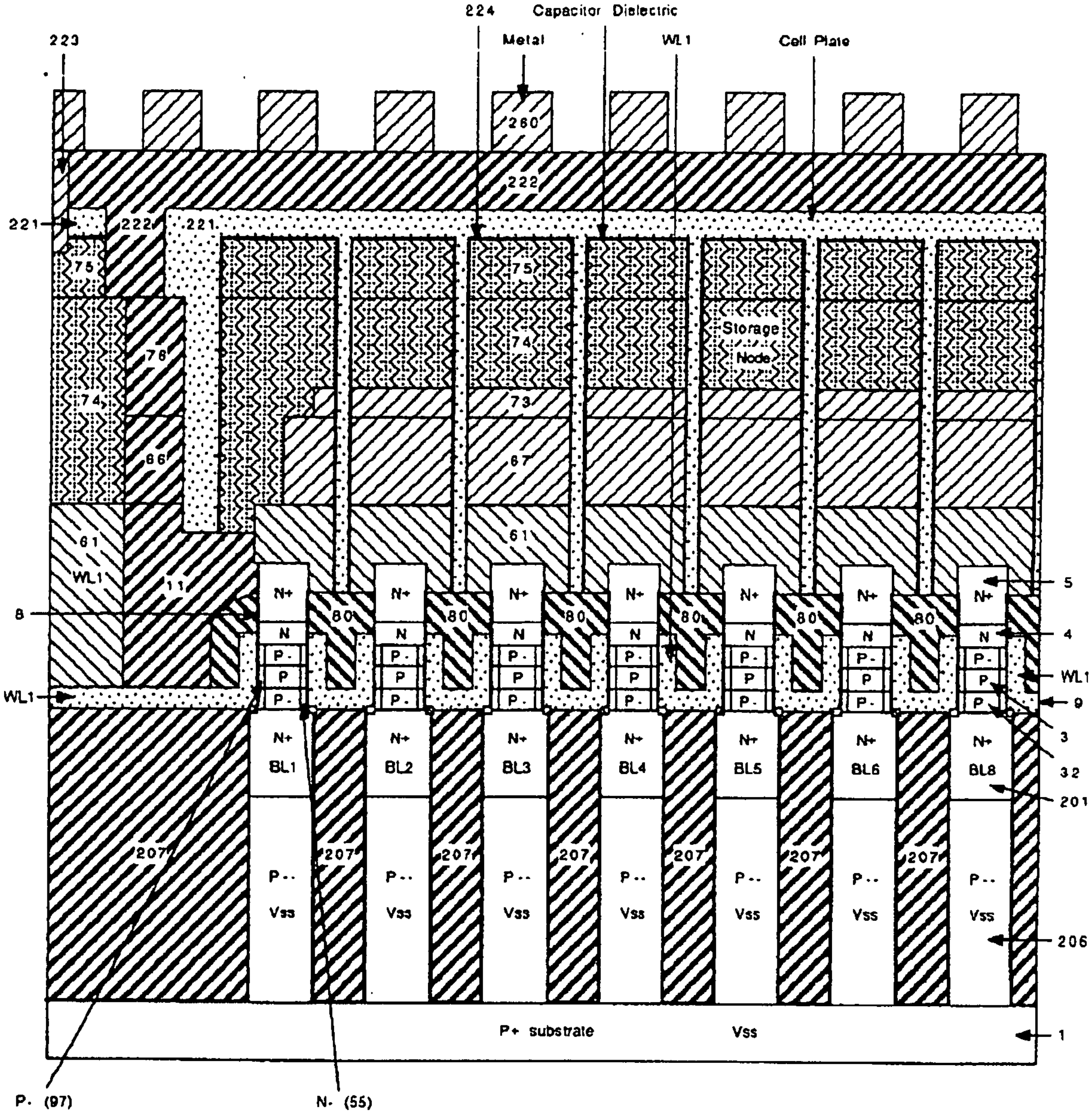
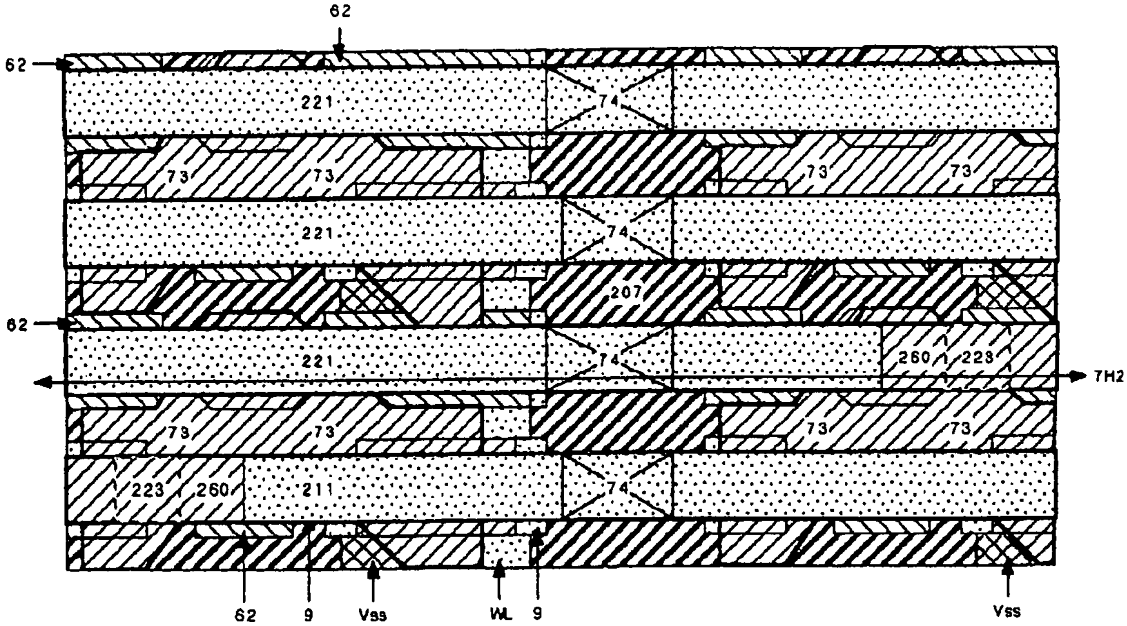


Fig.7H

Memory Array (SRAM)



SRAM Cell Size = 10 X 4 lithographic squares

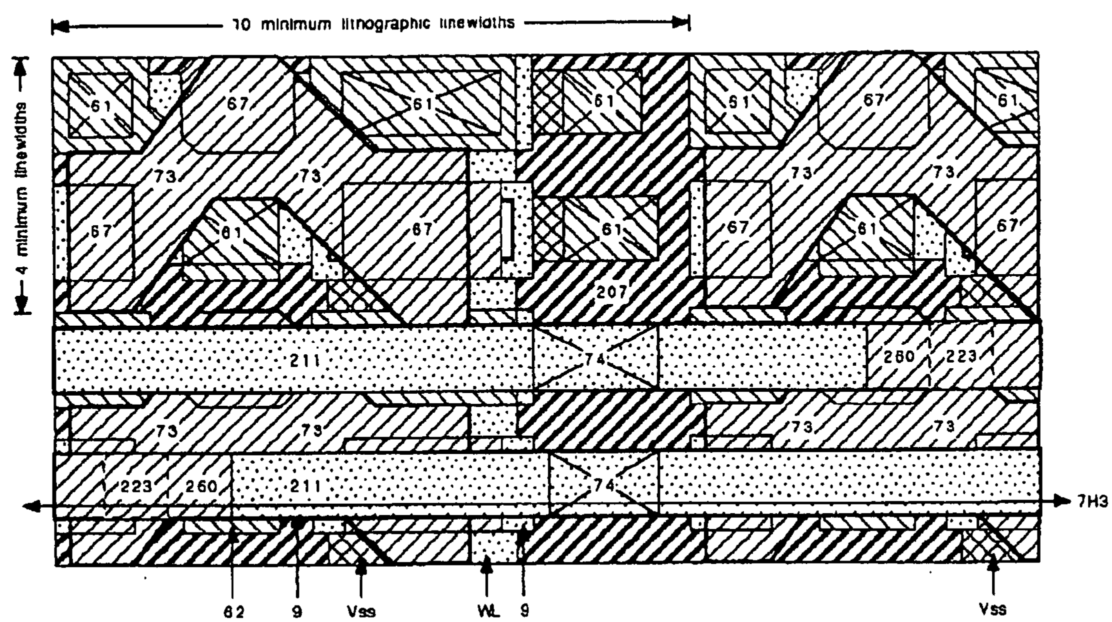


Fig.7H1

Memory Array (SRAM)

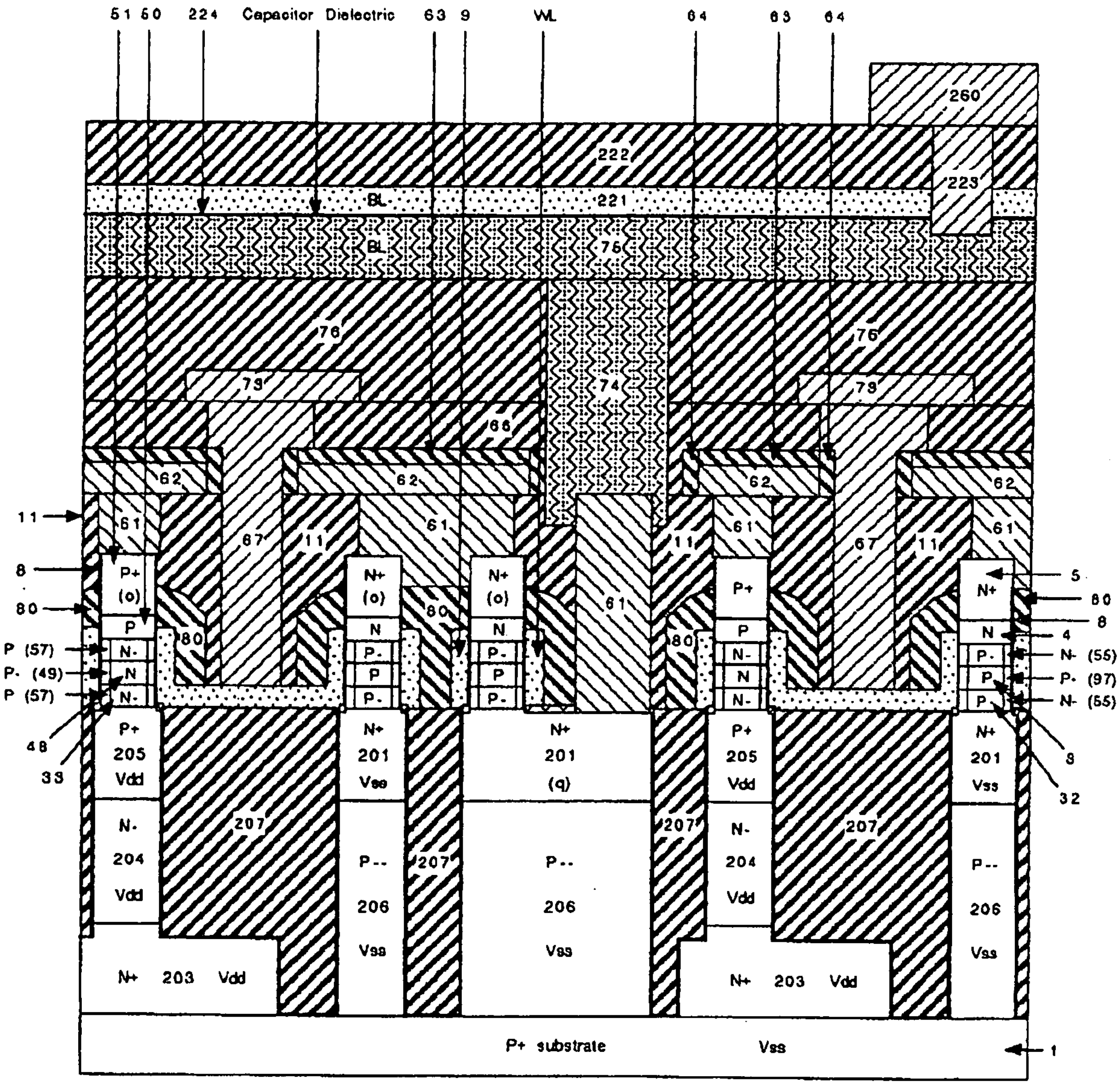


Fig.7H2

Memory Array (SRAM)

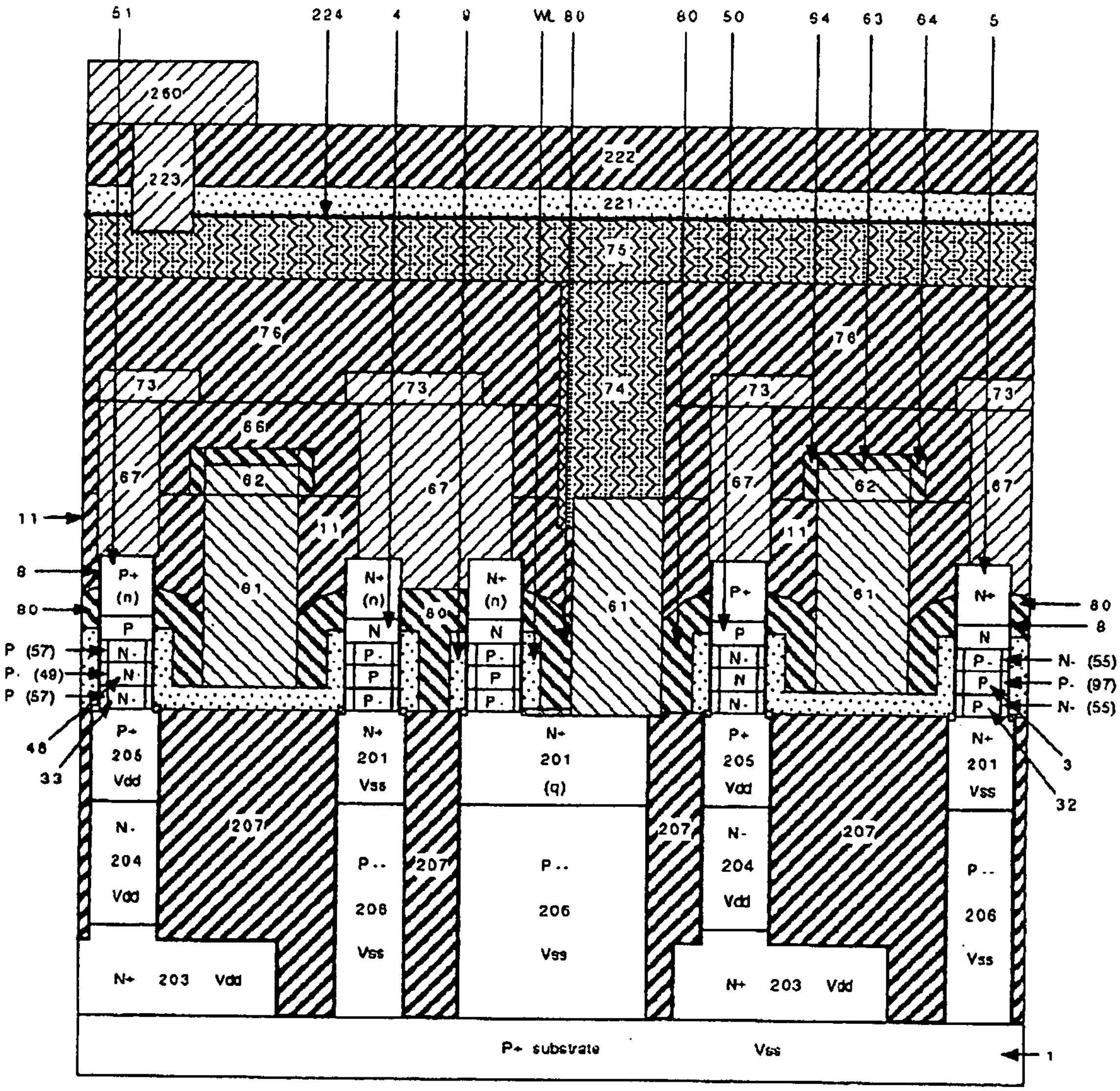


Fig.7H3

Logic Circuits (A Full Adder)

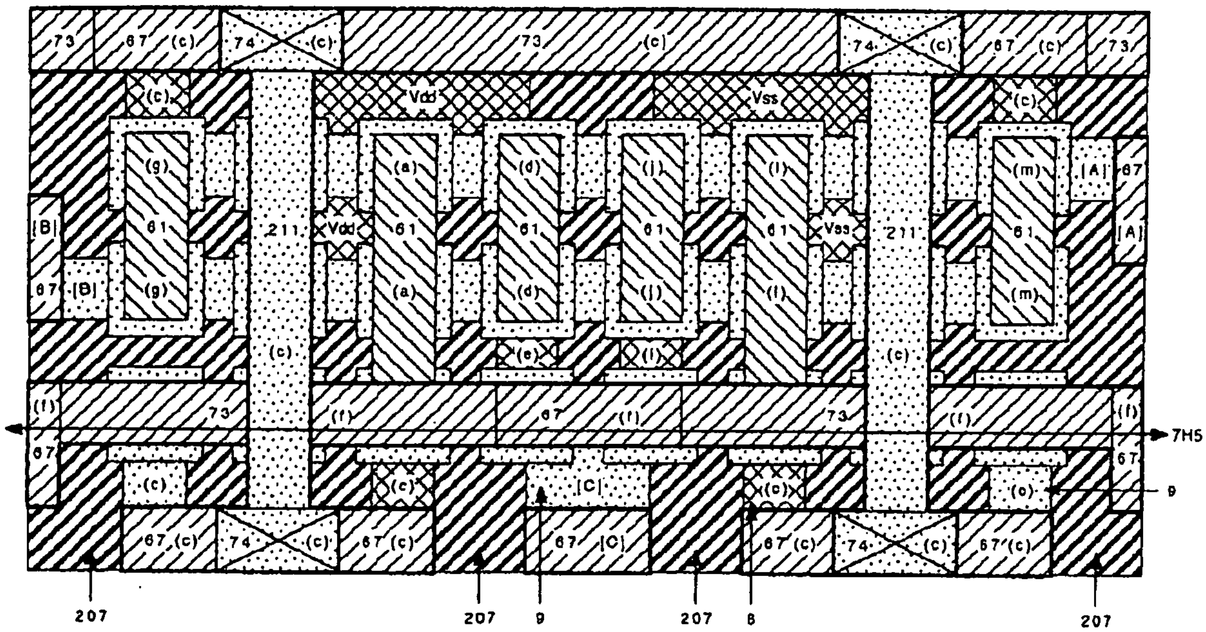


Fig.7H4

Logic Circuits (A Full Adder)

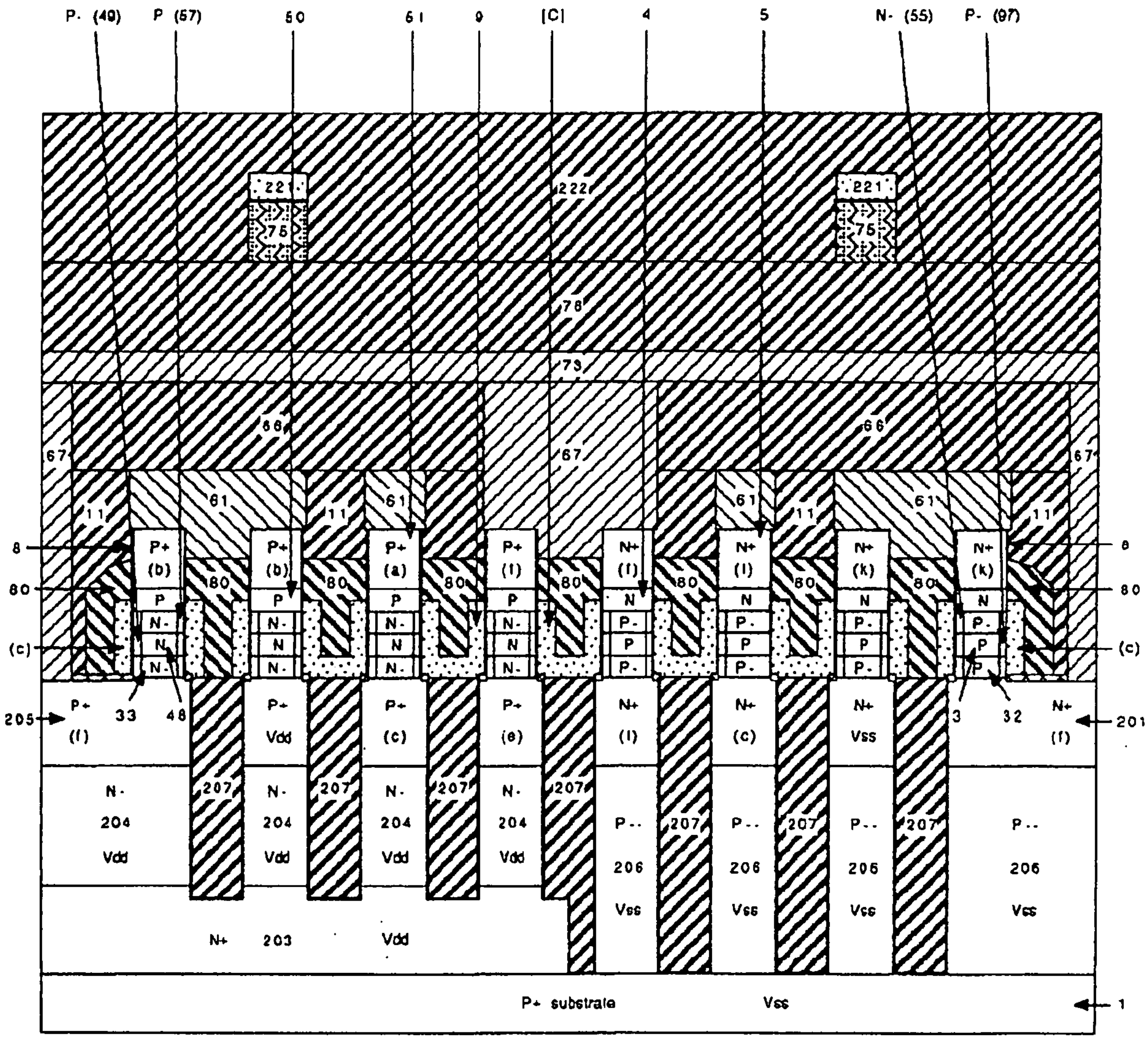


Fig.7H5

Logic circuits (CMOS flip-flop)

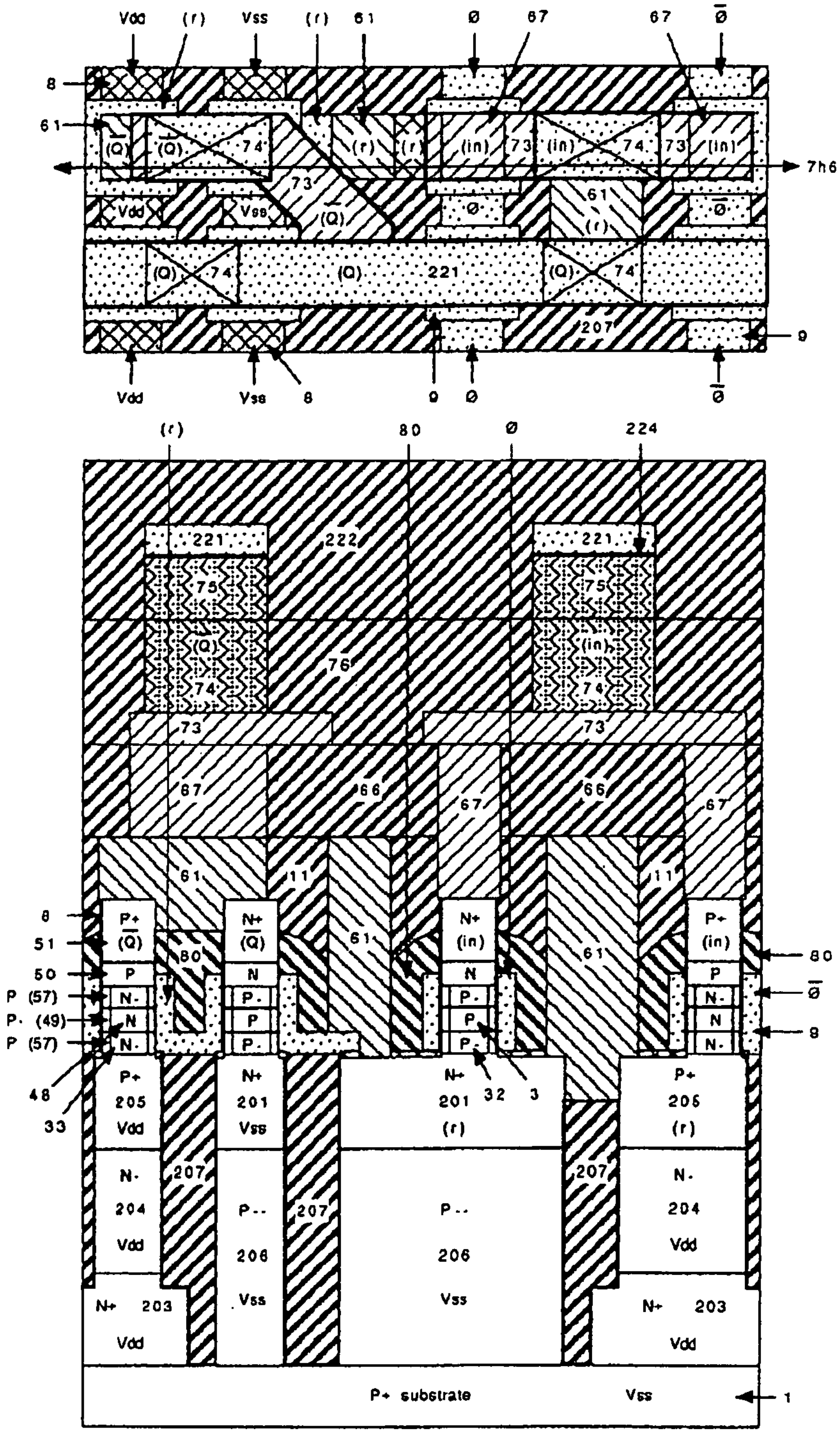


Fig.7H6

Logic circuits (CMOS flip-flop)

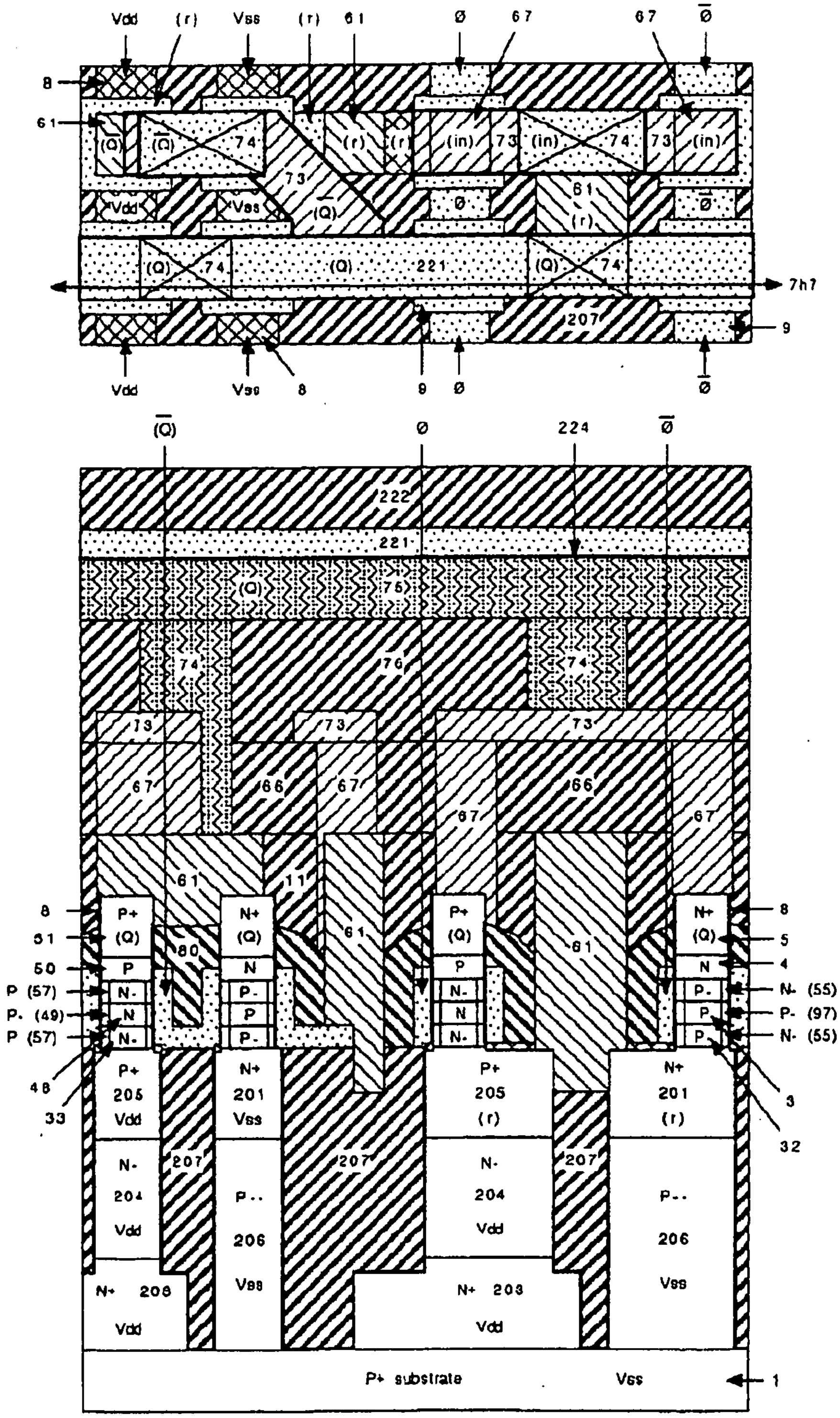


Fig.7H7

Logic circuits (CMOS NAND)

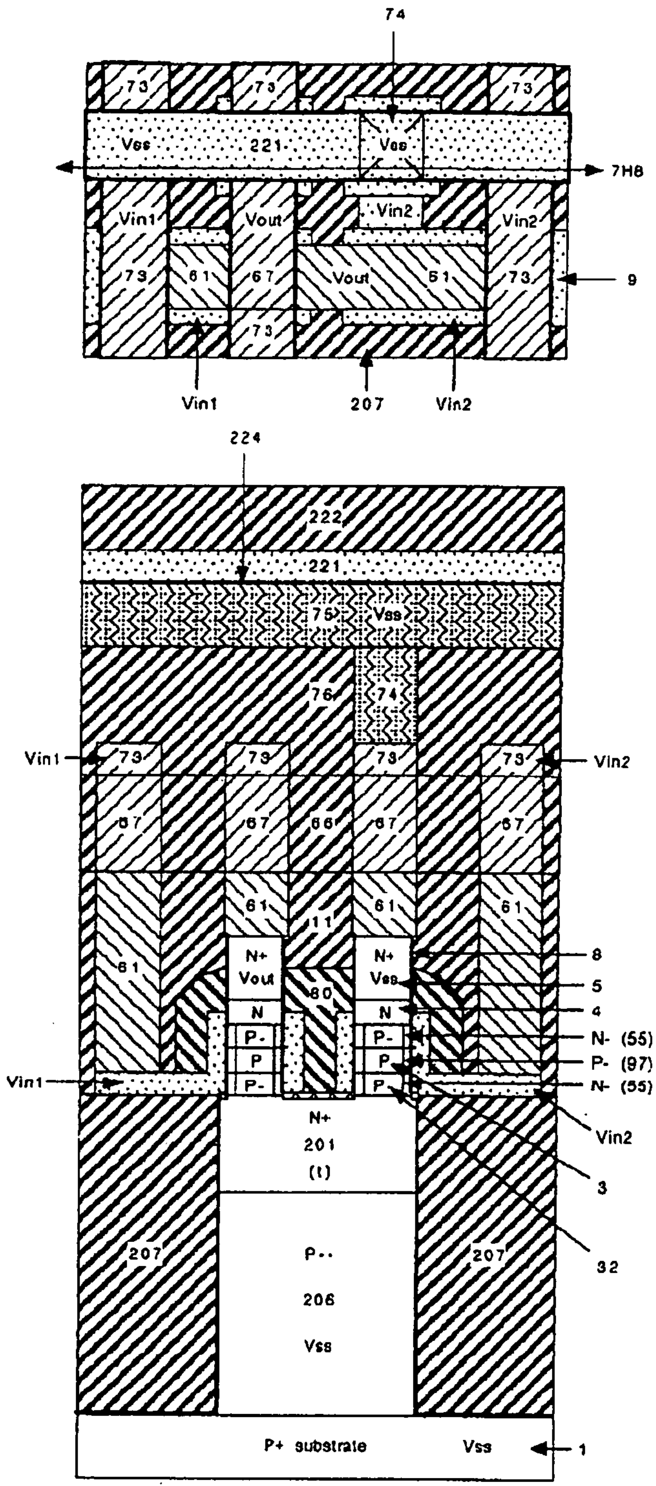


Fig.7H8

Logic circuits (CMOS NAND)

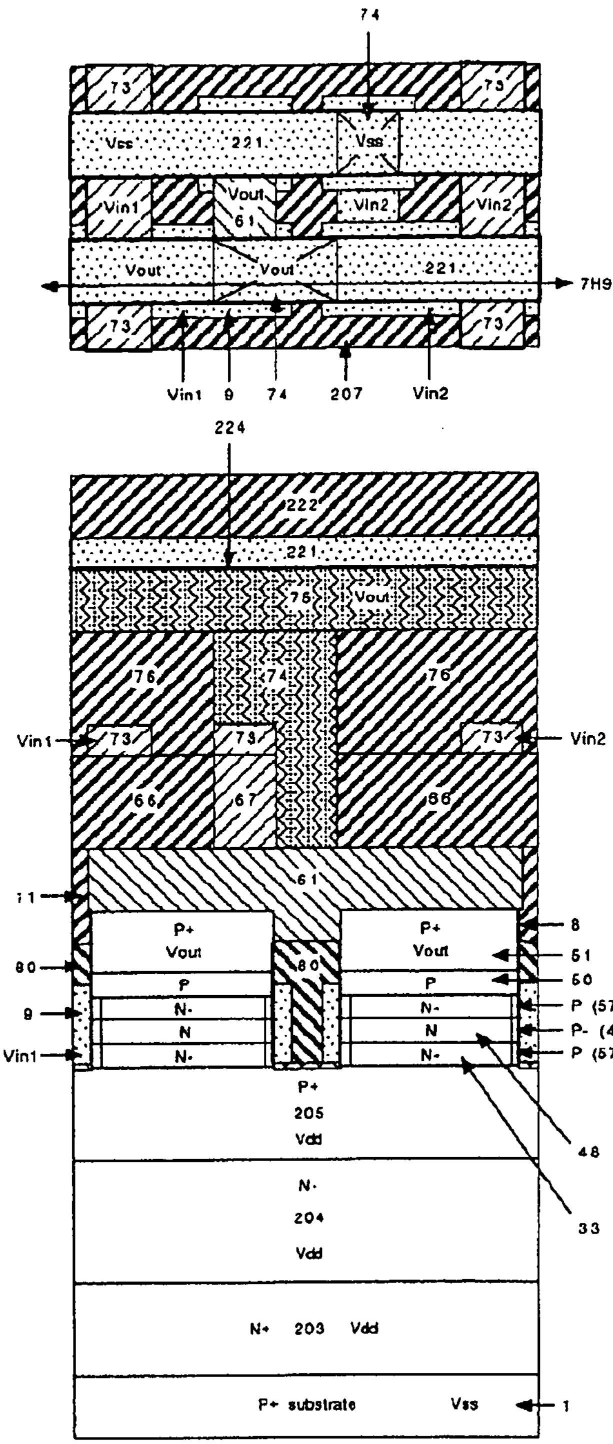


Fig.7H9

Logic circuits (CMOS NAND)

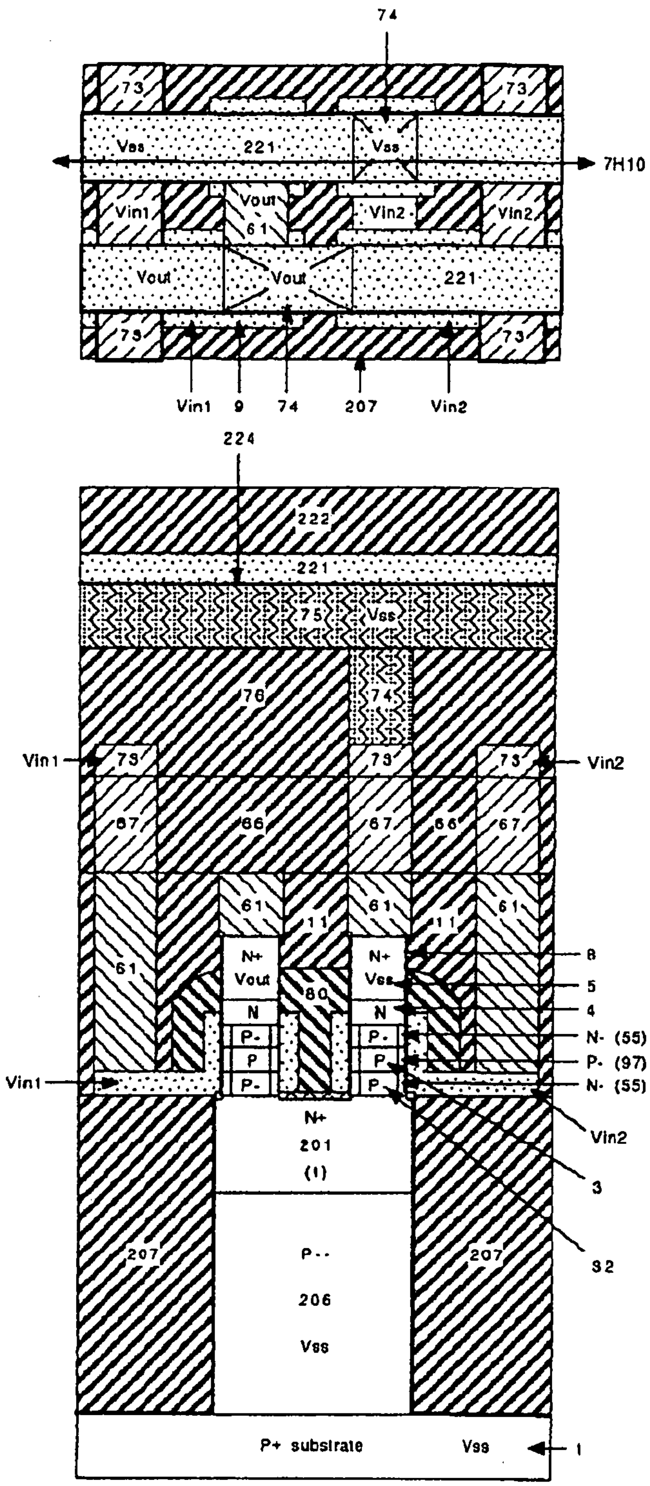


Fig.7H10

Memory Array (DRAM)

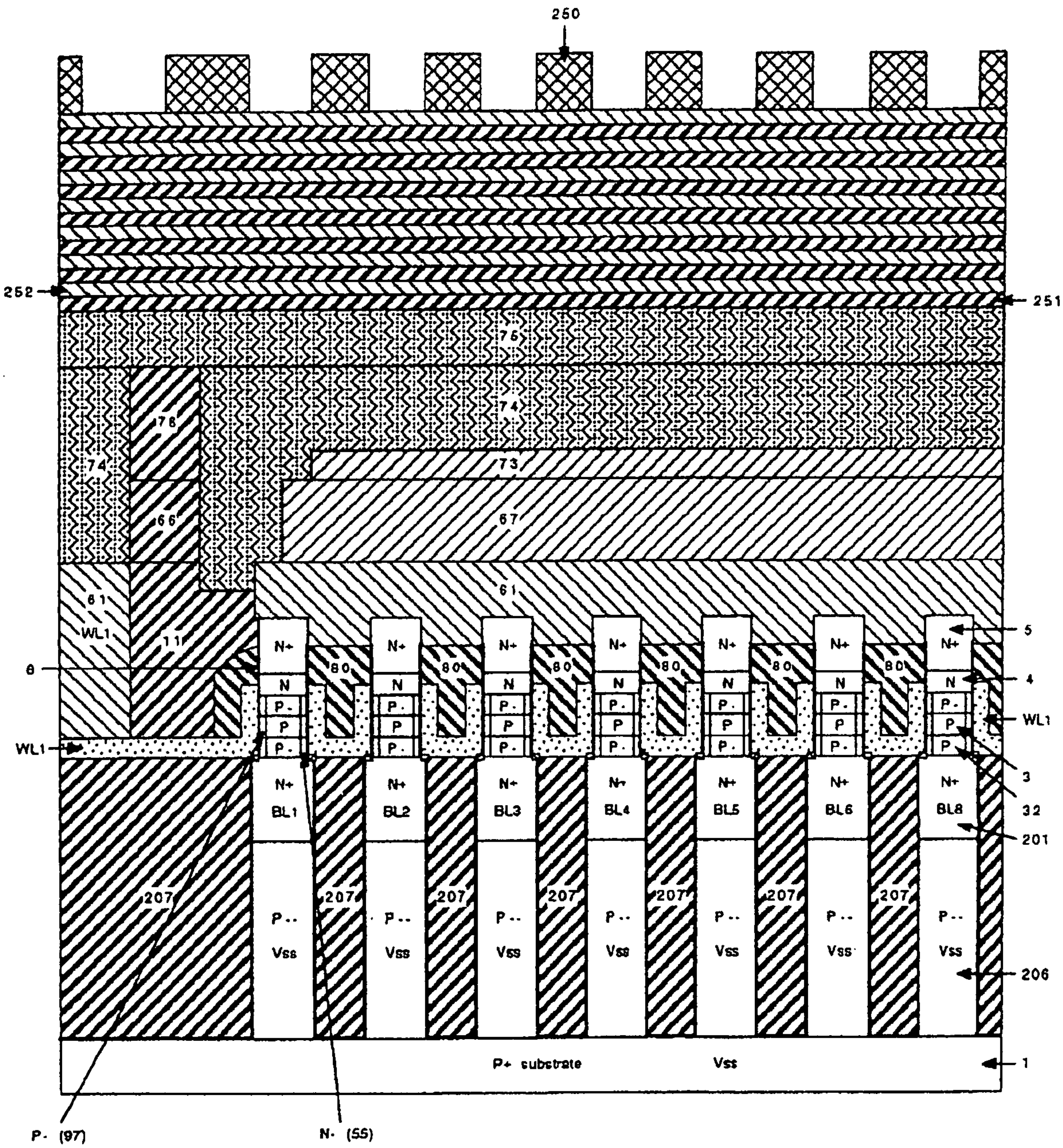


Fig.8A

Memory Array (DRAM)

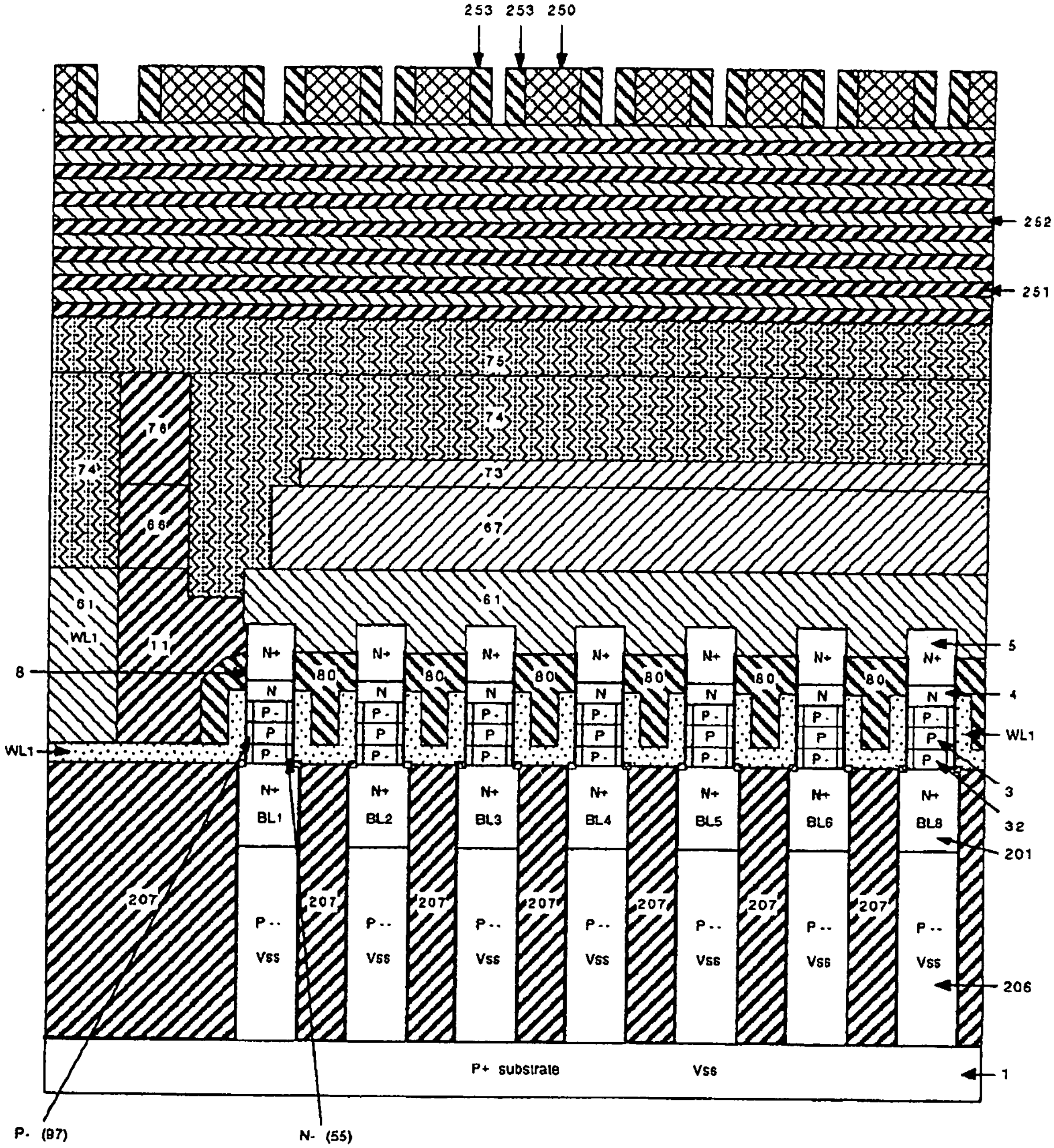


Fig.8B

Memory Array (DRAM)

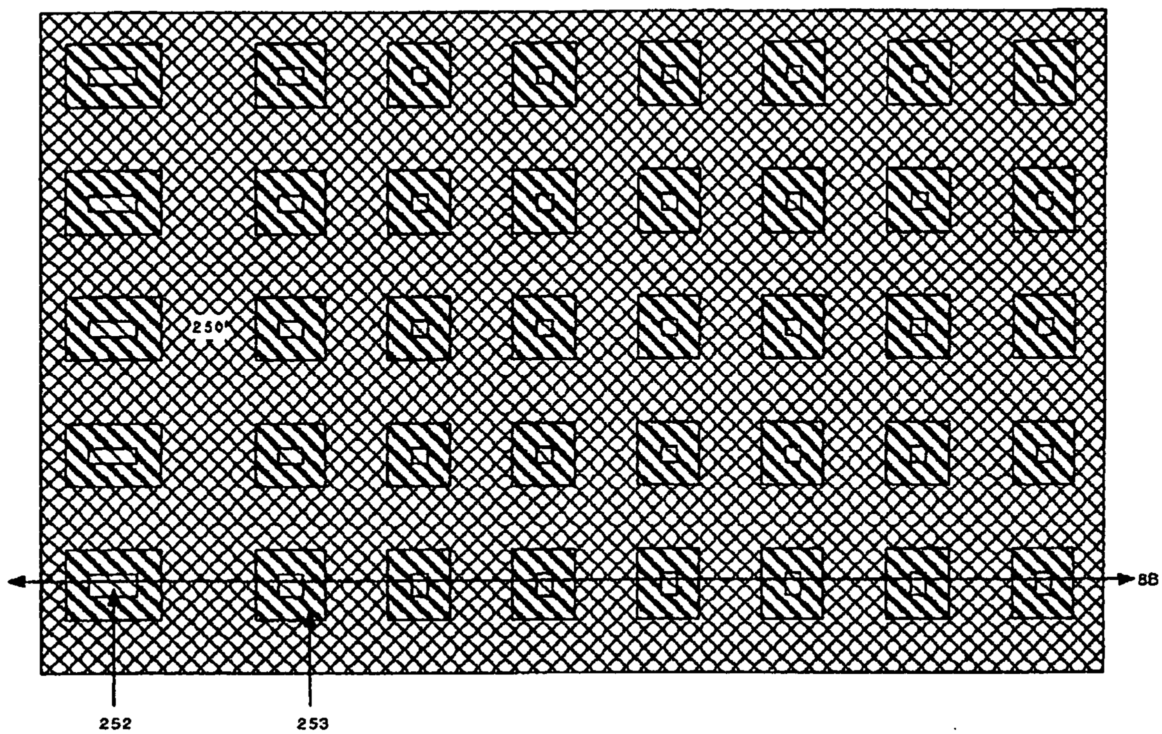


Fig.8B1

Memory Array (DRAM)

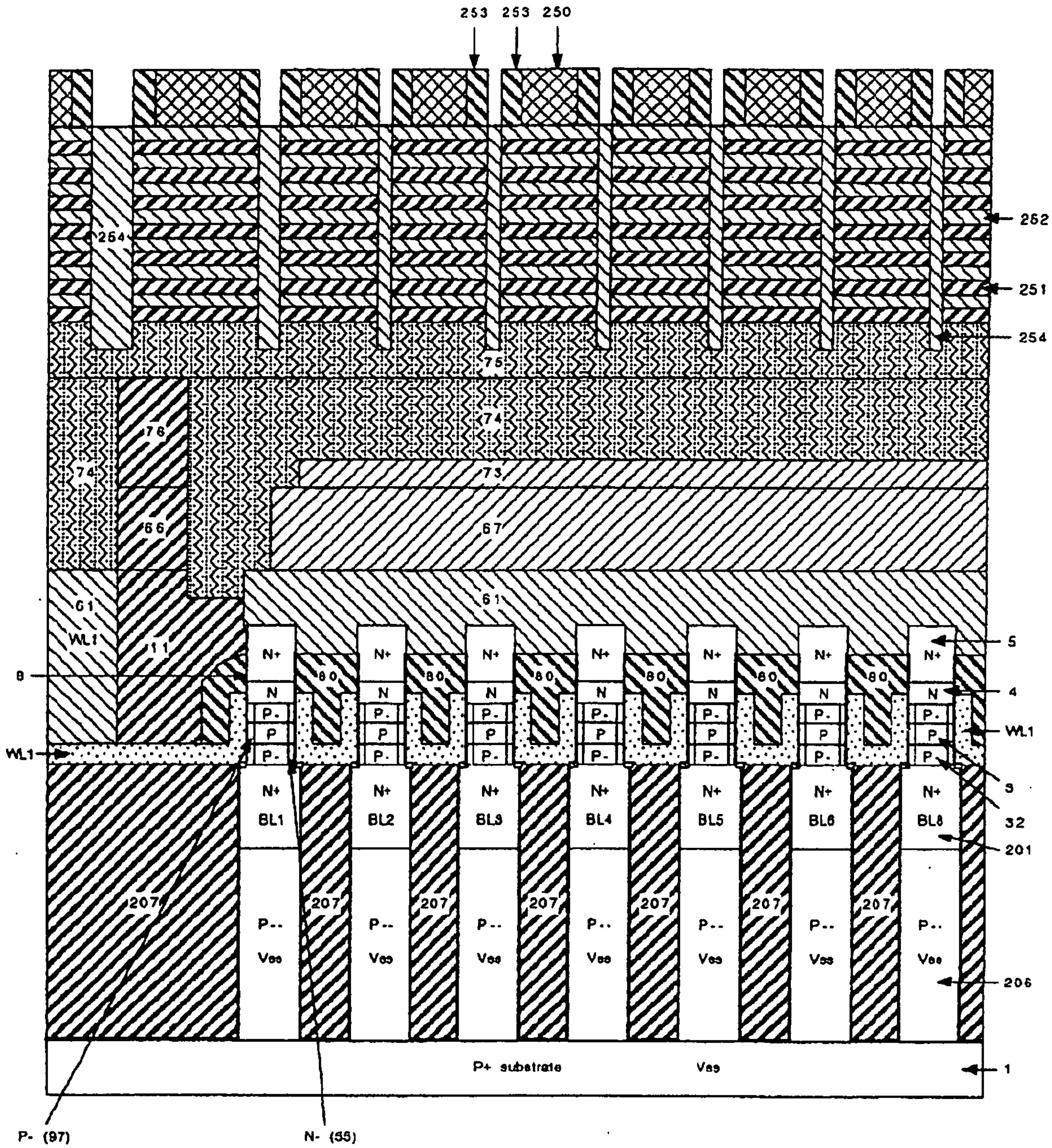


Fig.8C

Memory Array (DRAM)

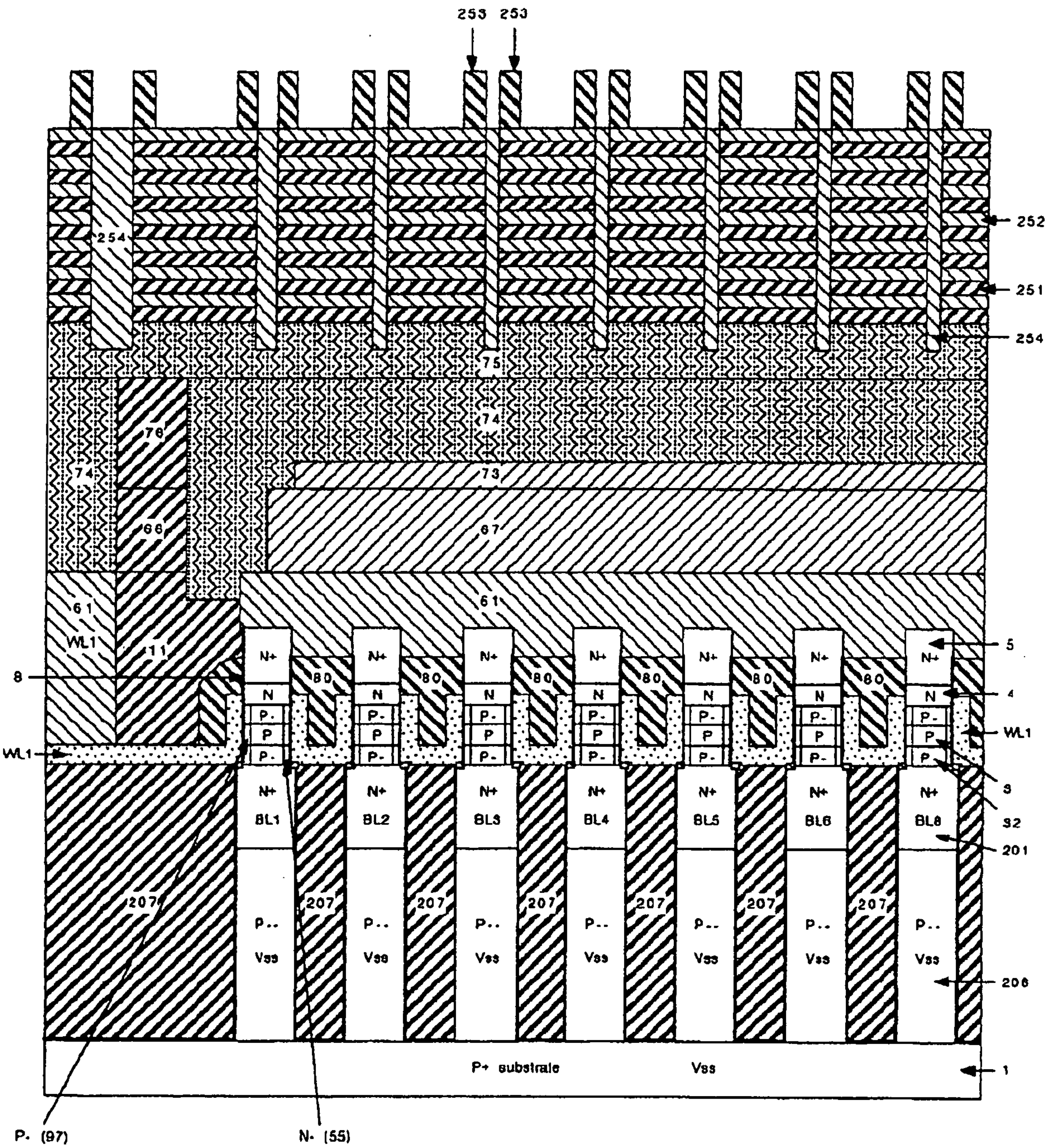


Fig.8D

Memory Array (DRAM)

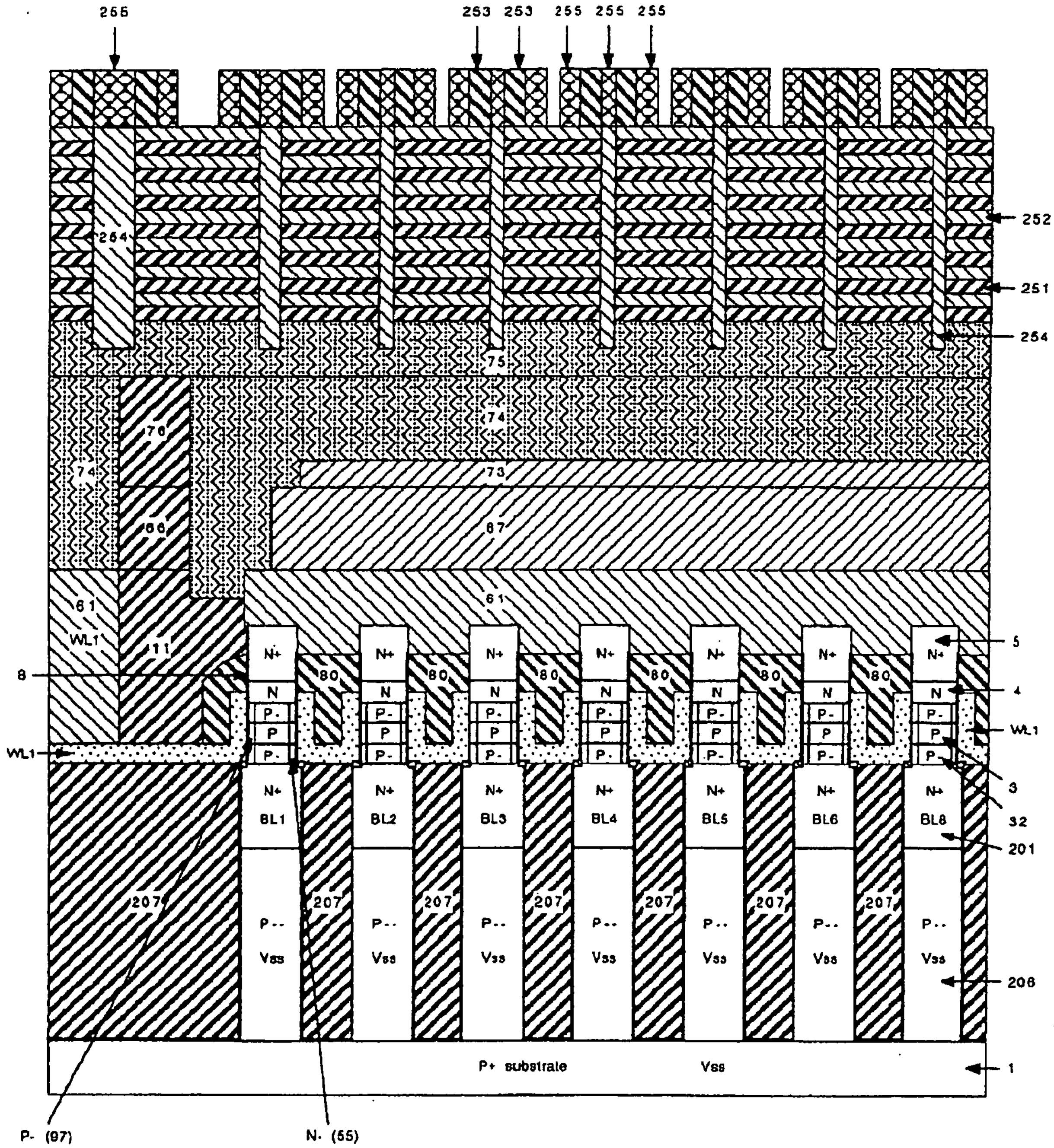


Fig.8E

Memory Array (DRAM)

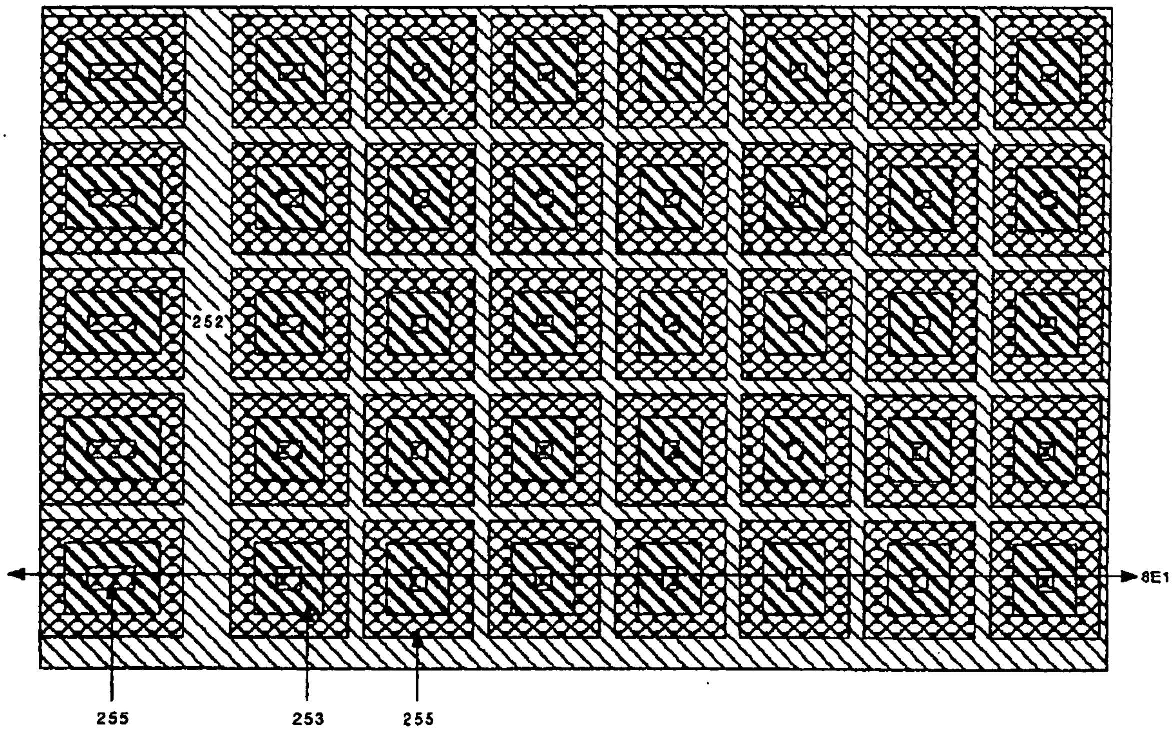


Fig.8E1

Memory Array (DRAM)

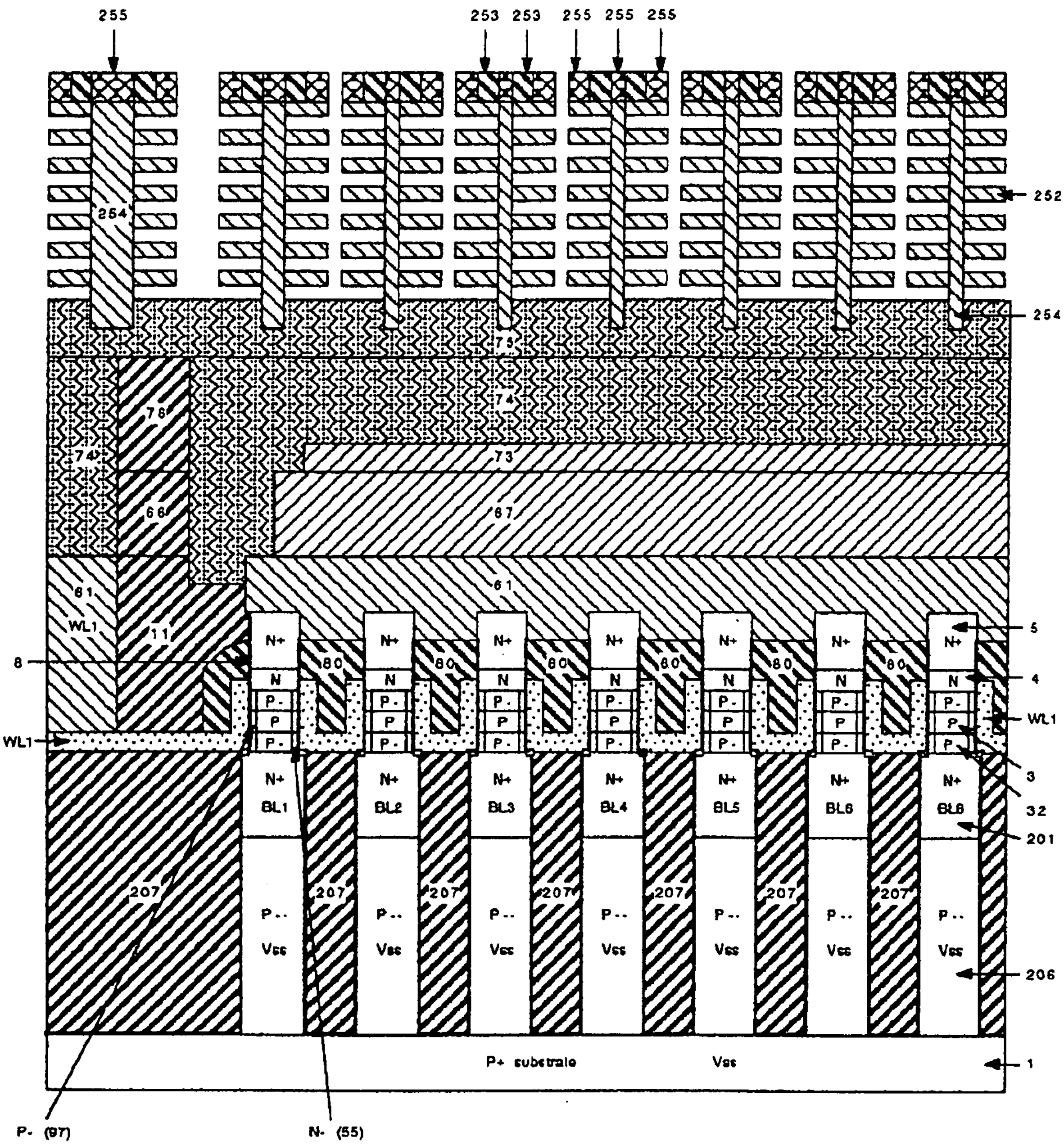


Fig.8F

Memory Array (DRAM)

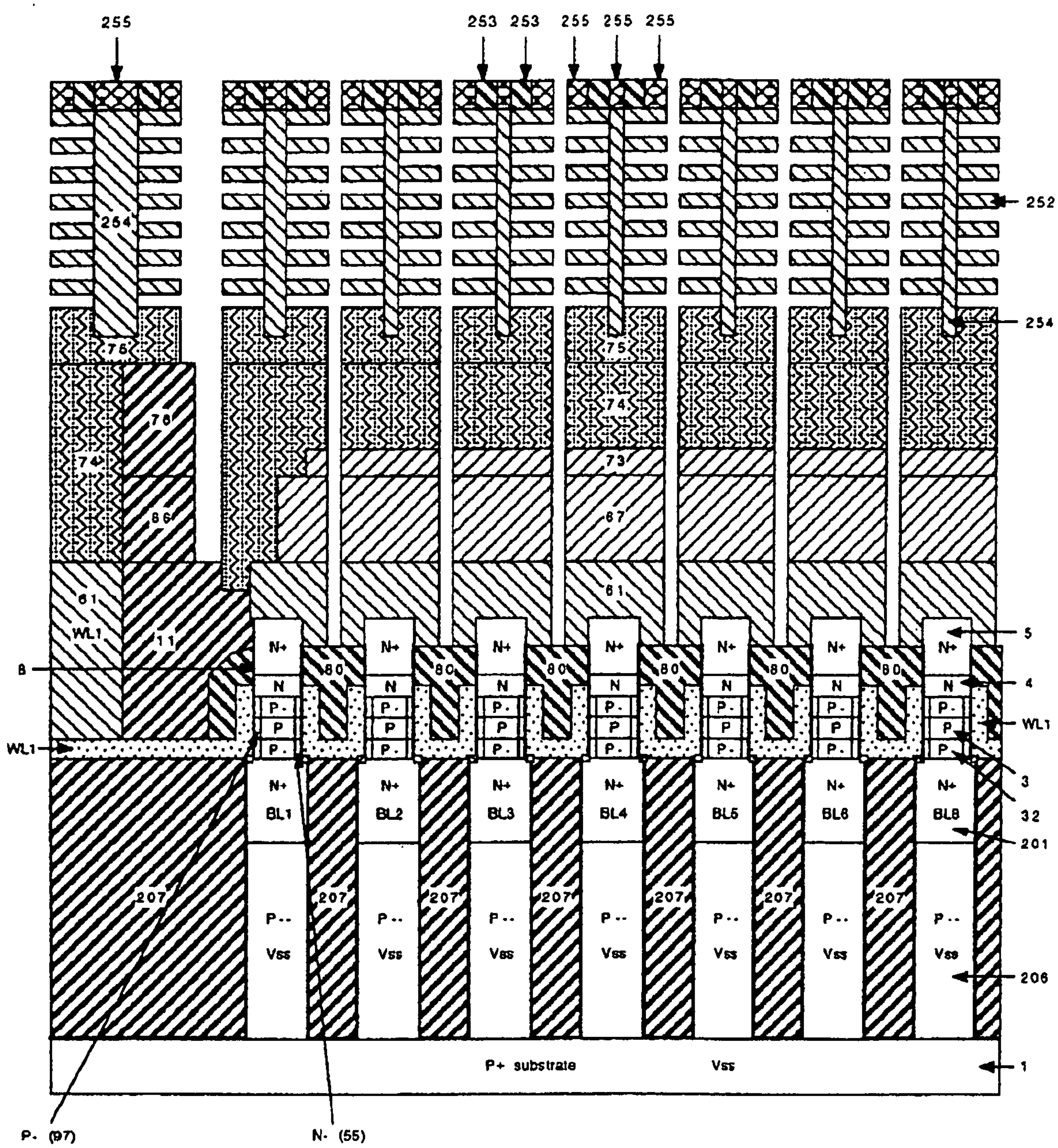


Fig.8G

Memory Array (DRAM)

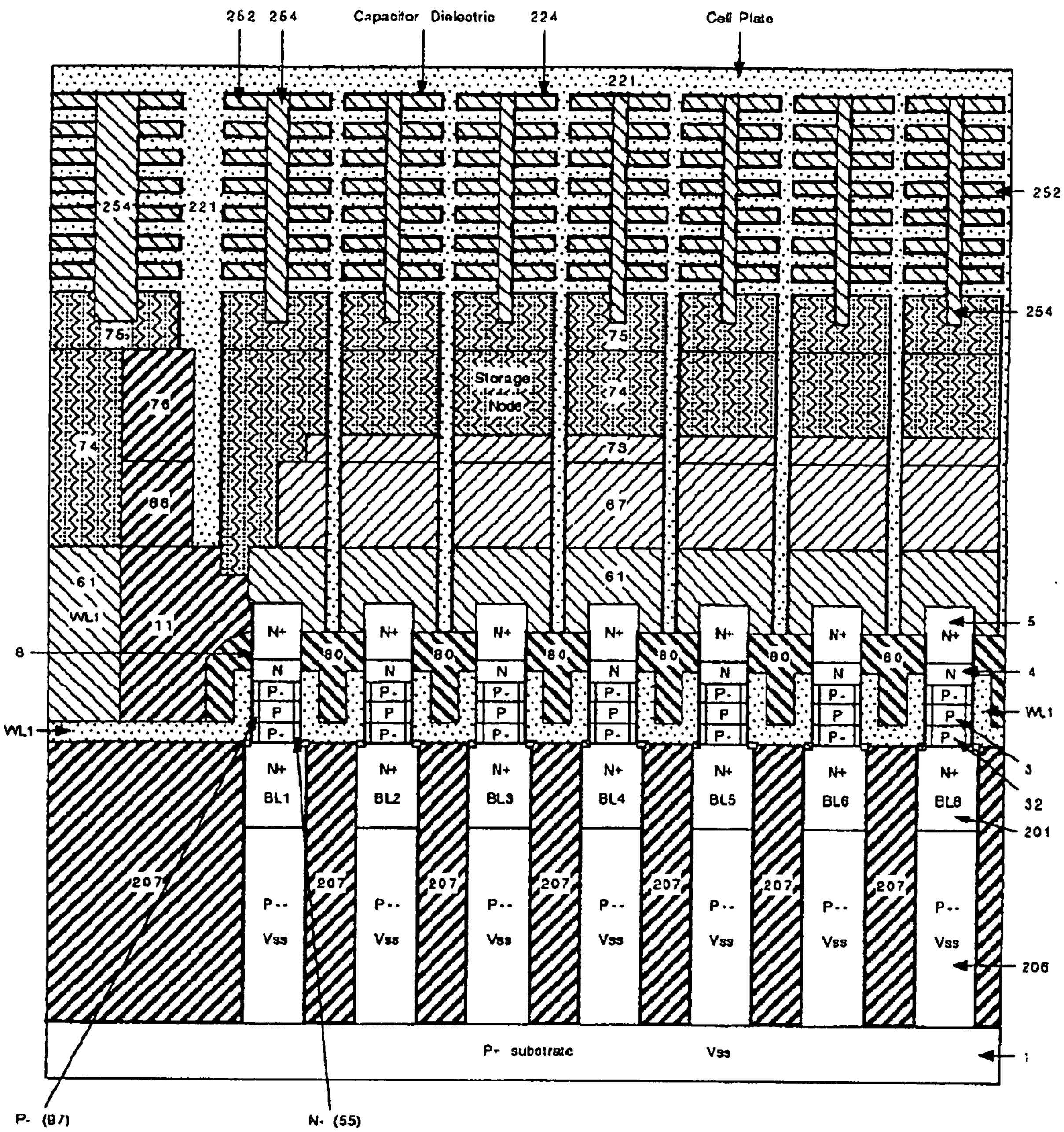


Fig.8H

Memory Array (DRAM)

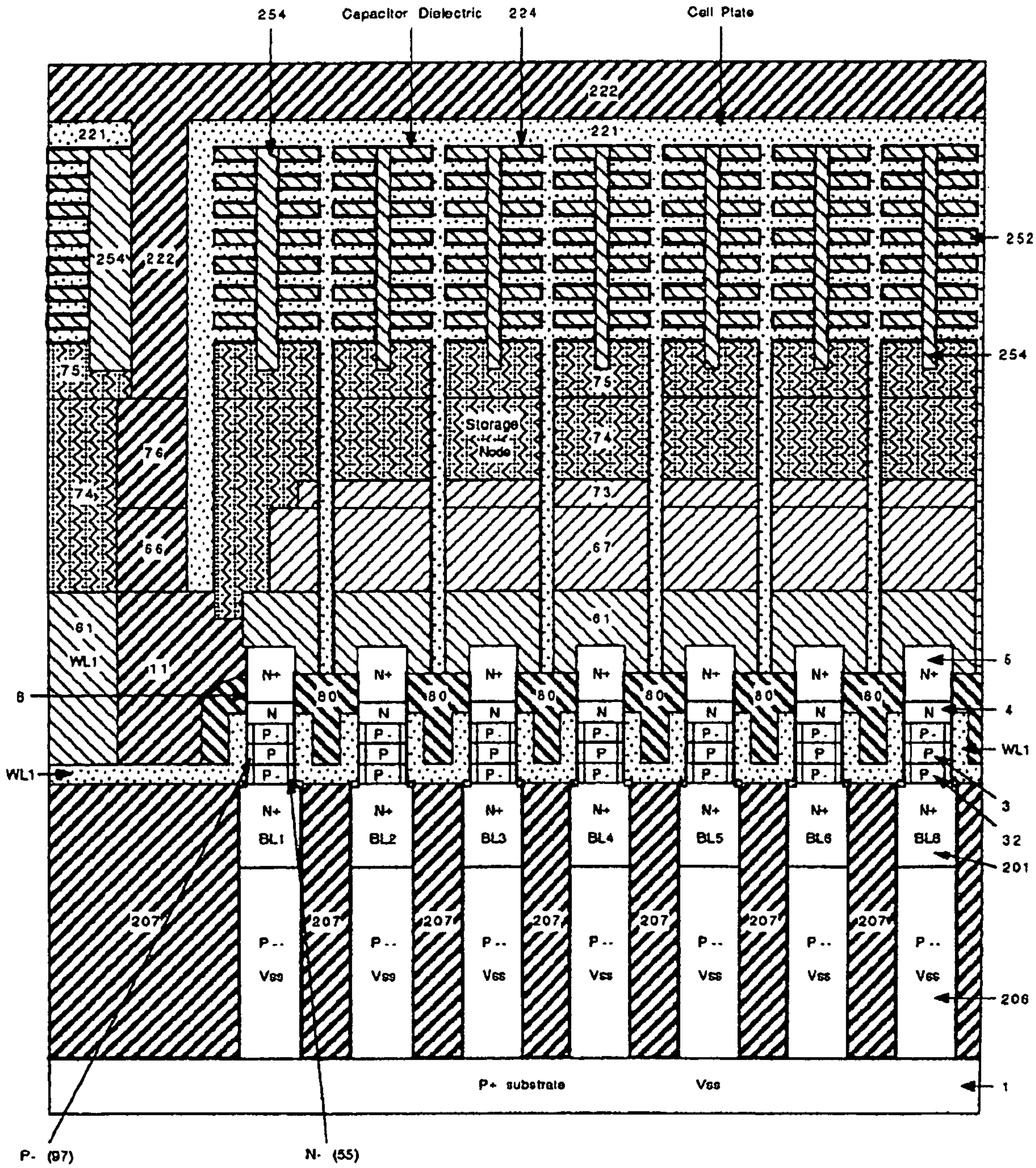


Fig.8I

Memory Array (DRAM)

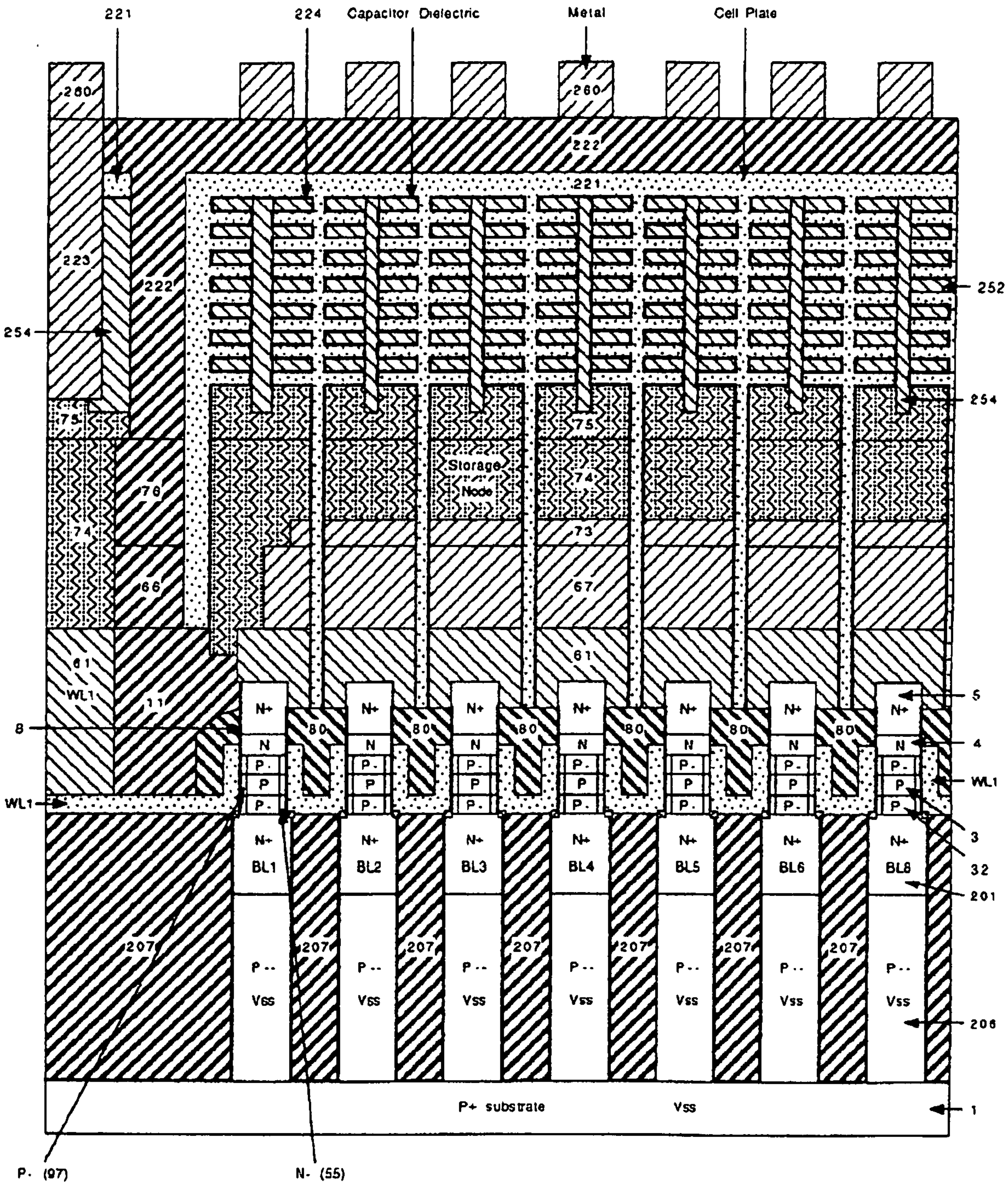


Fig.8J

Memory Array (DRAM)

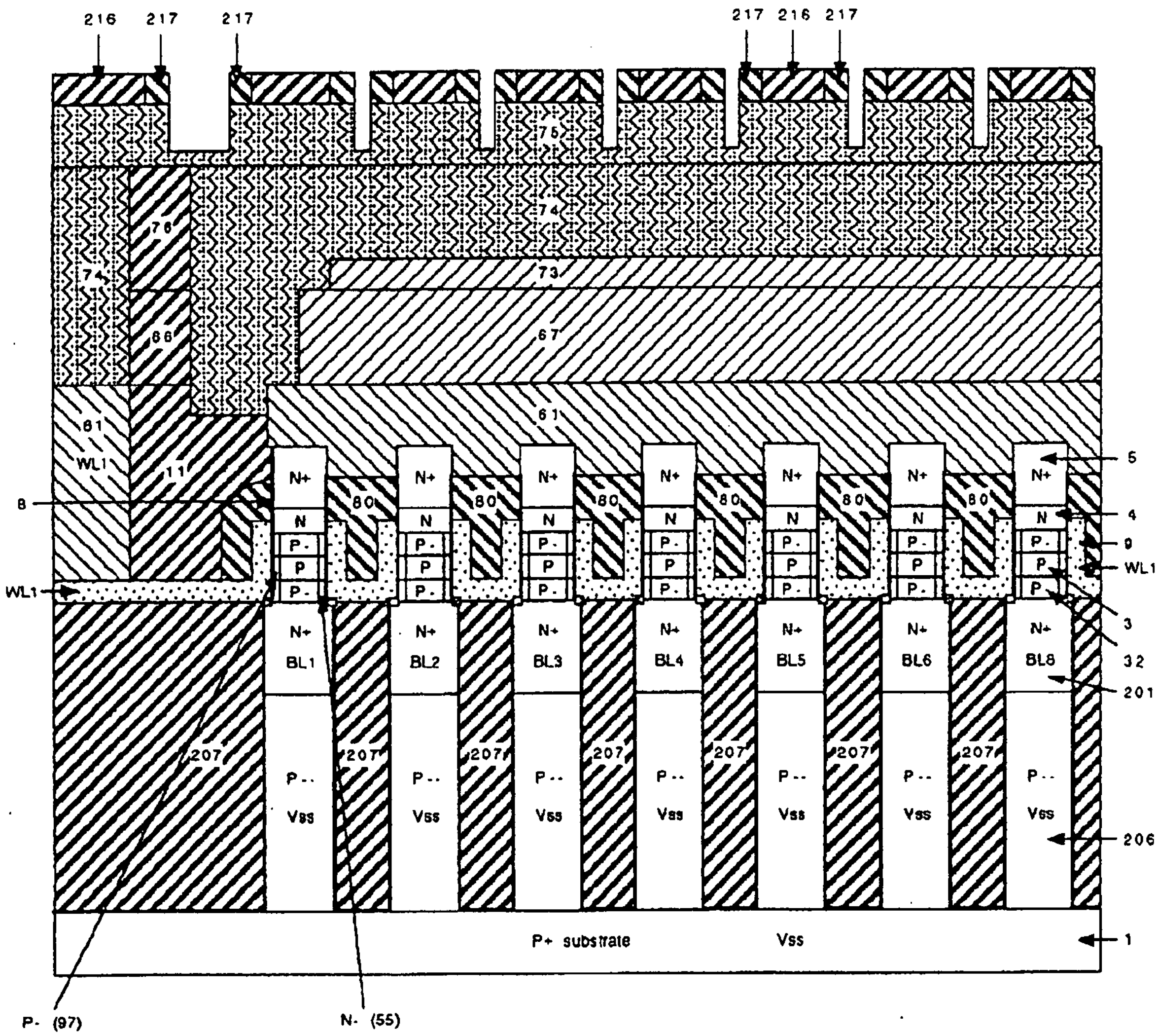


Fig.8K

Memory Array (DRAM)

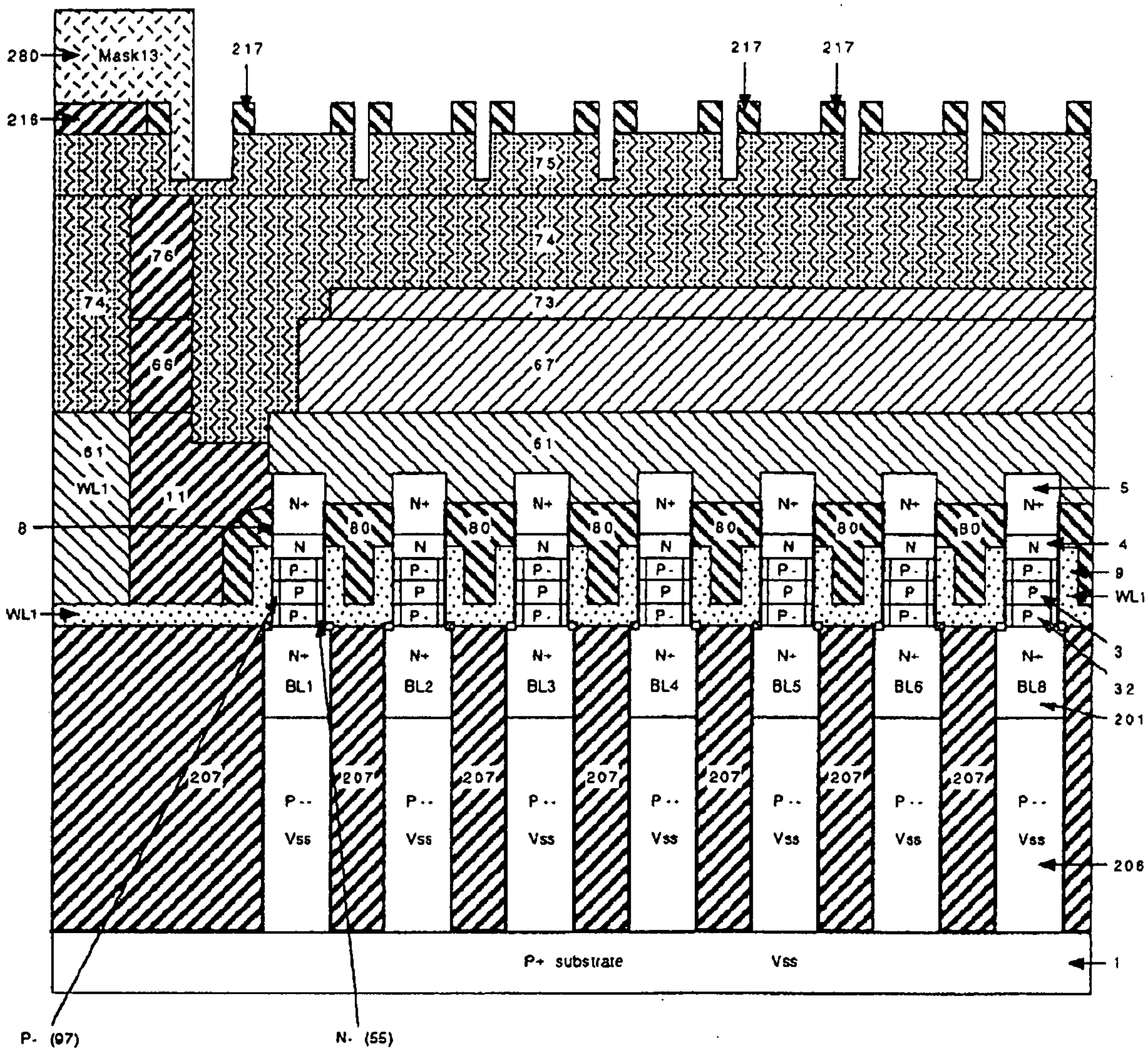


Fig.8L

Memory Array (DRAM)

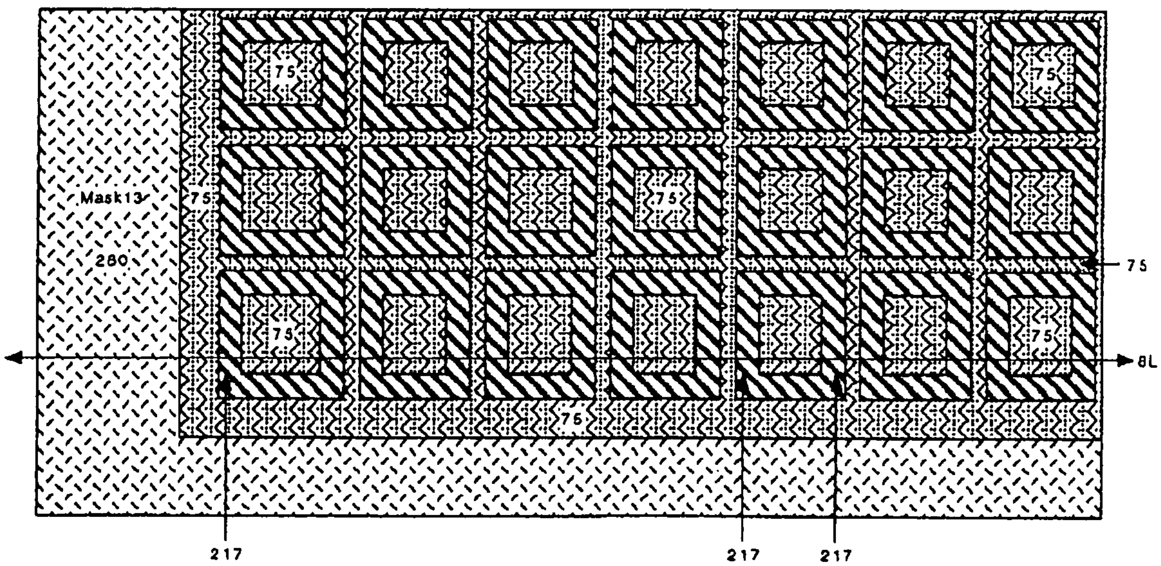


Fig.8L1

Memory Array (DRAM)

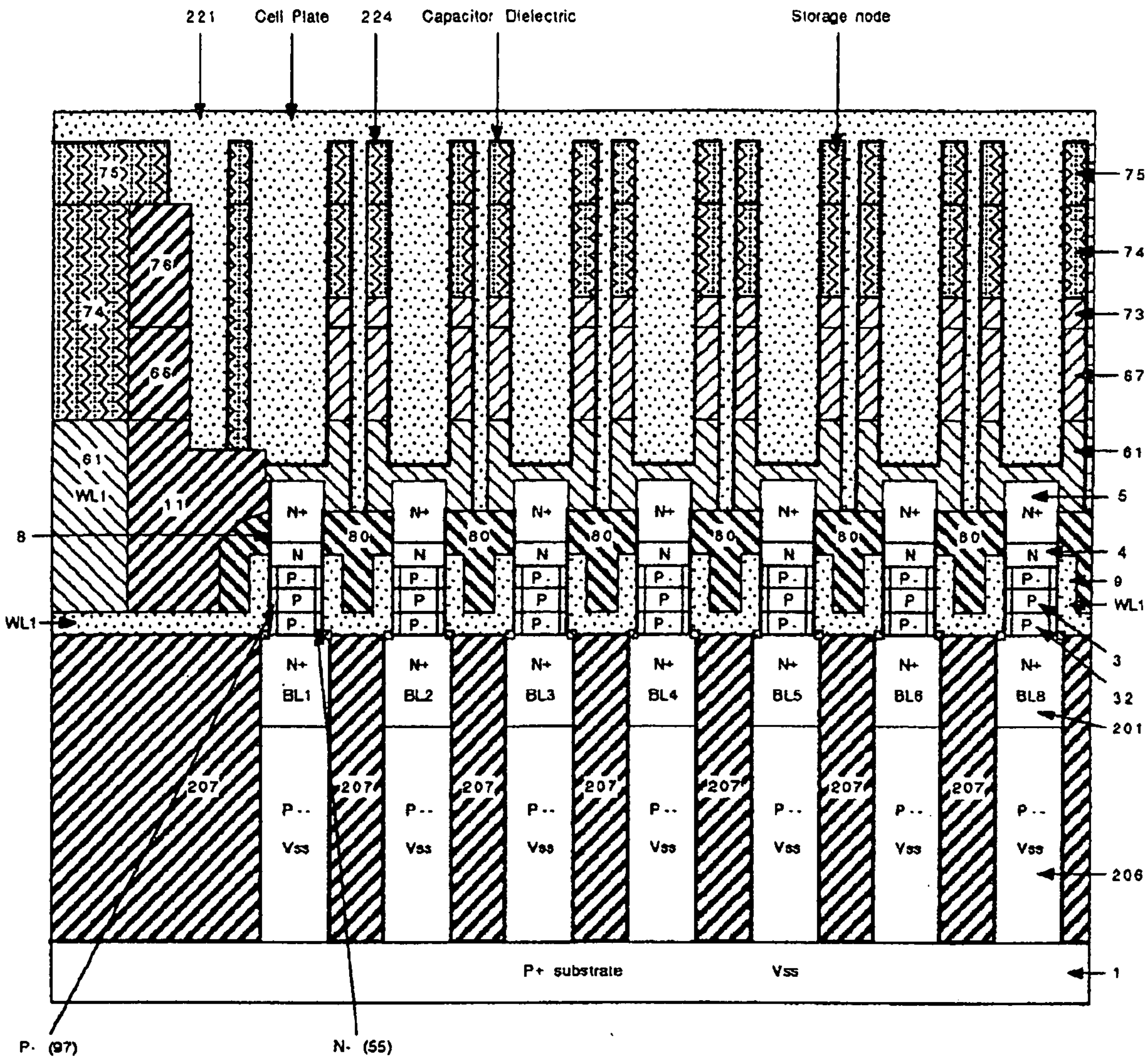


Fig.8M

Memory Array (DRAM)

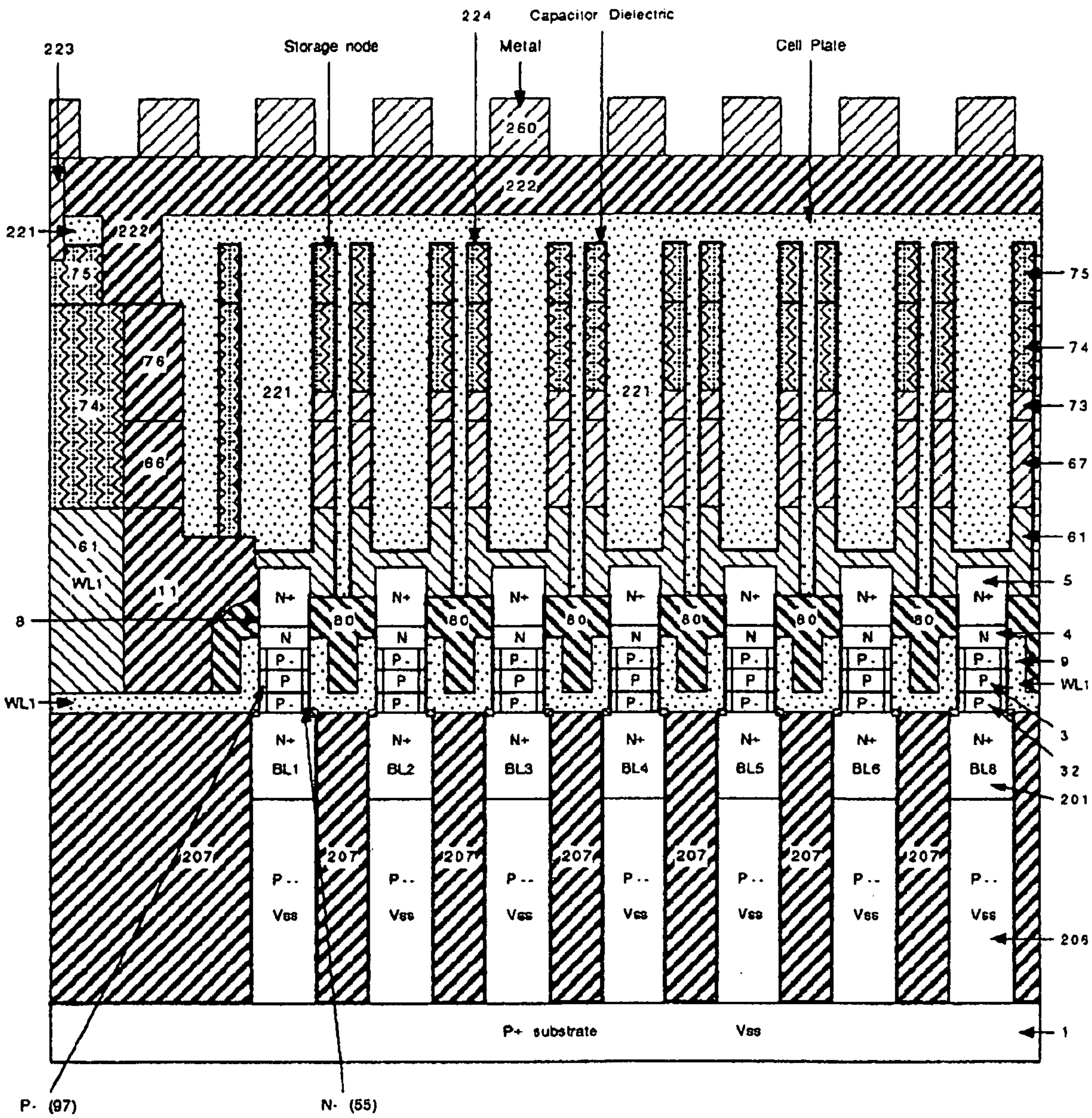


Fig.8N

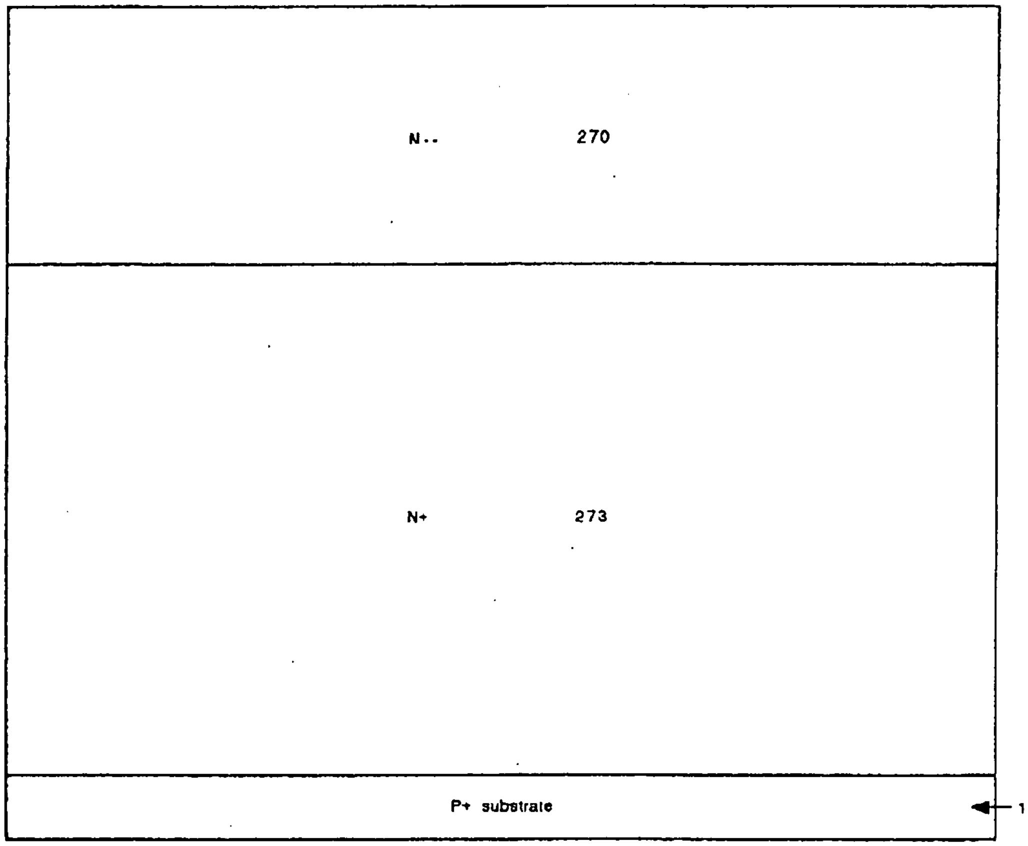


Fig.9A

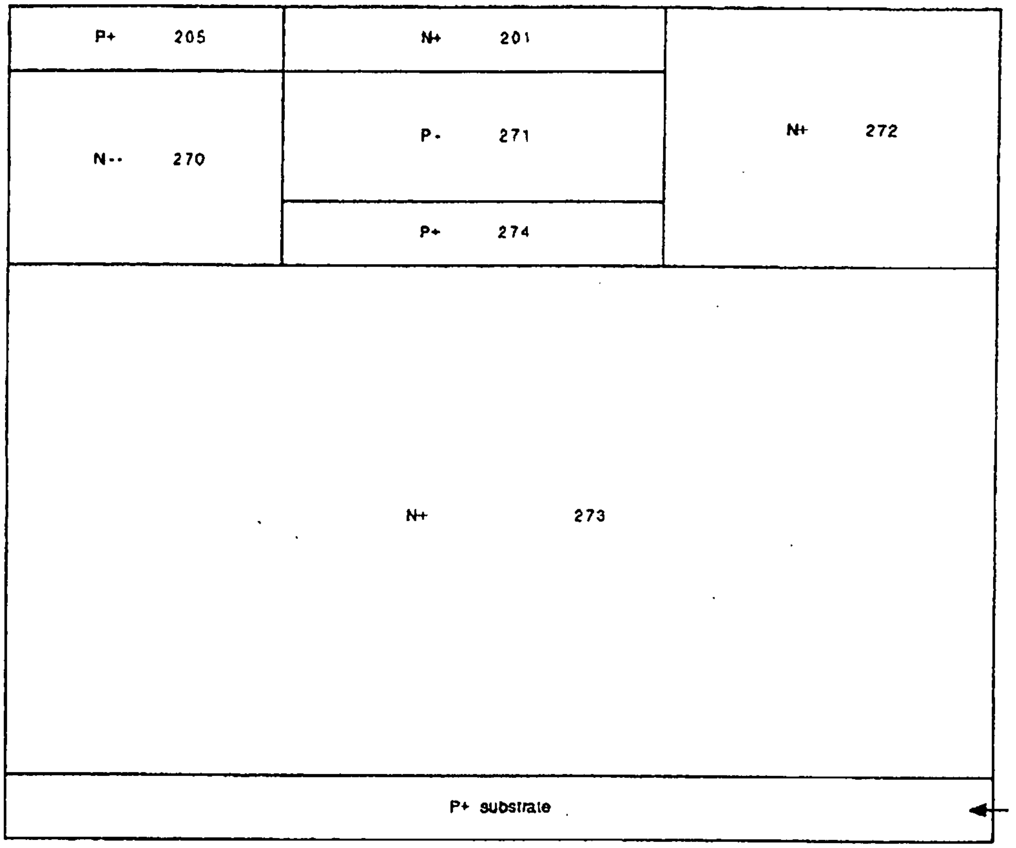


Fig.9B

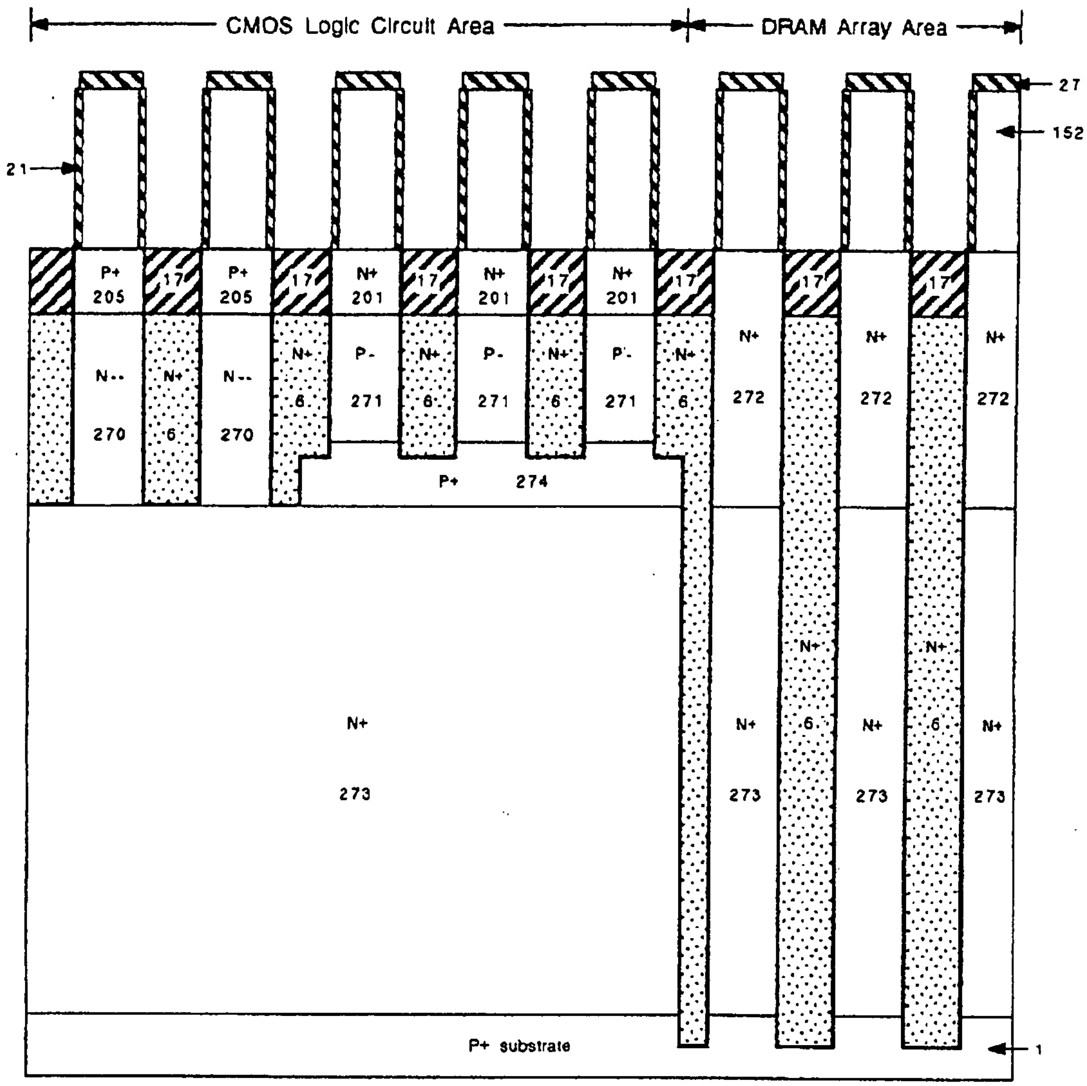

CMOS Logic Circuit Area
DRAM Array Area
27
152
21
P+
205
17
N+
201
N--
270
N+
6
P-
271
272
P+ 274
273
P+ substrate
1

Fig.9C

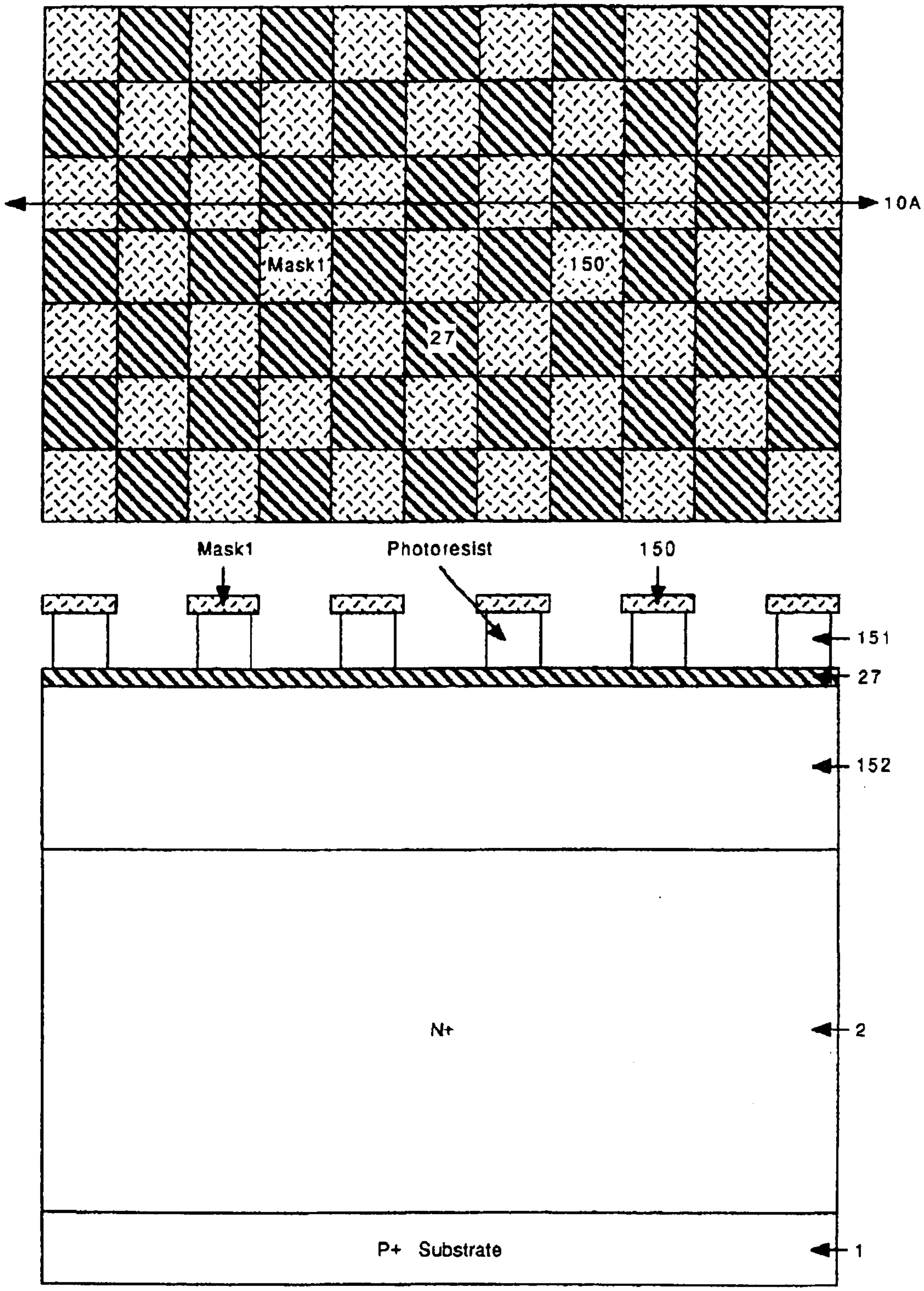
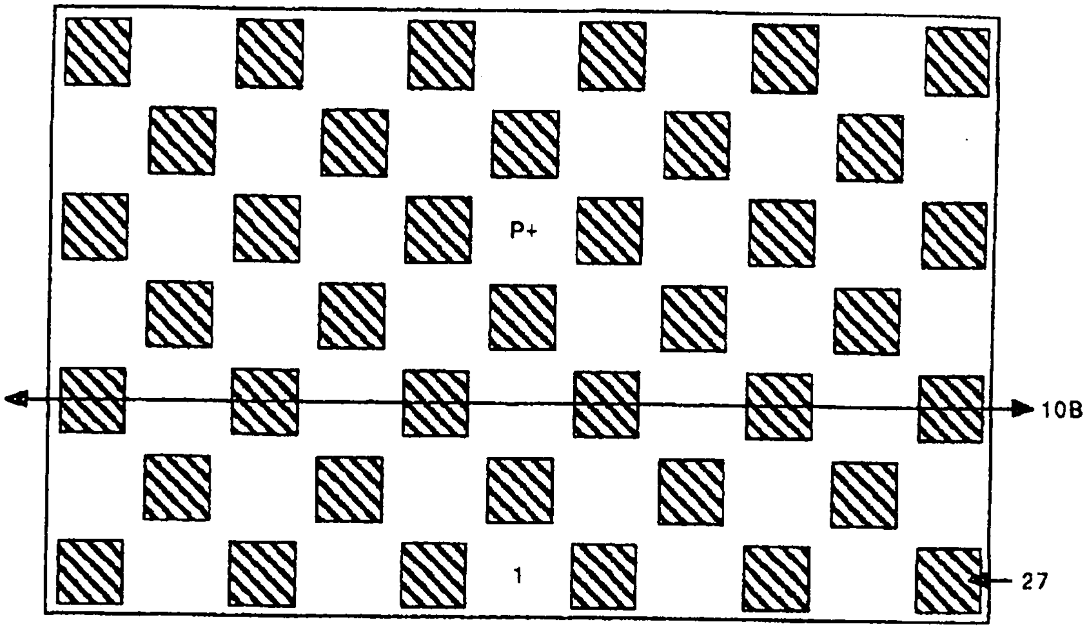

10A
Mask1
150
27
Mask1
Photoresist
150
151
27
152
N+
2
P+ Substrate
1

Fig.10A



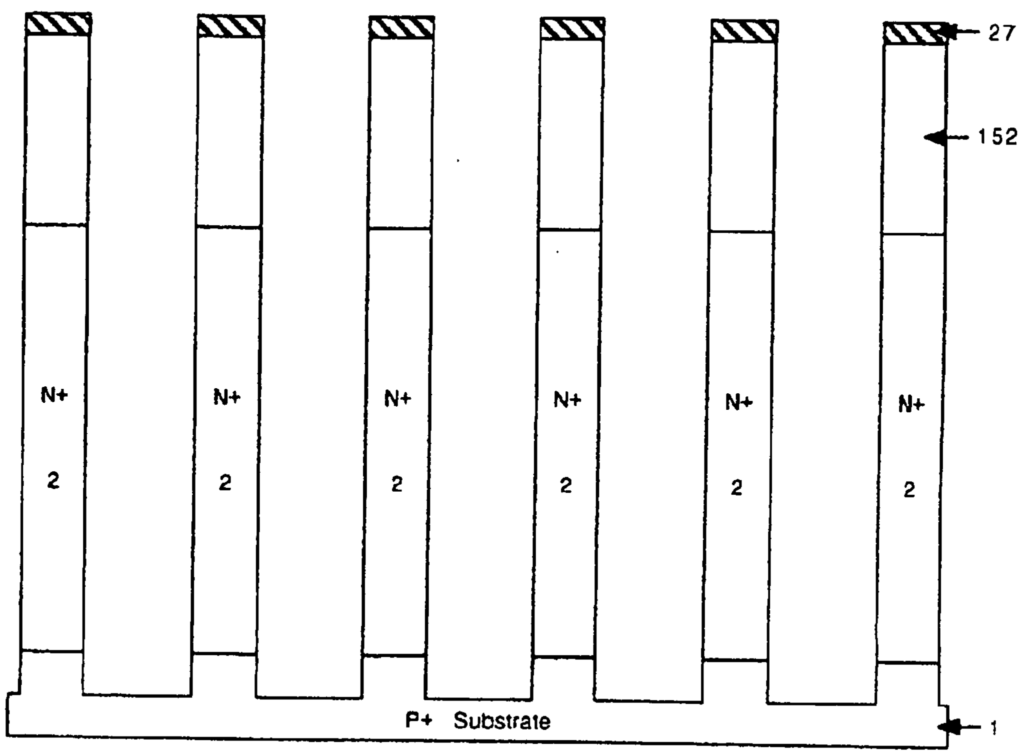


Fig.10B

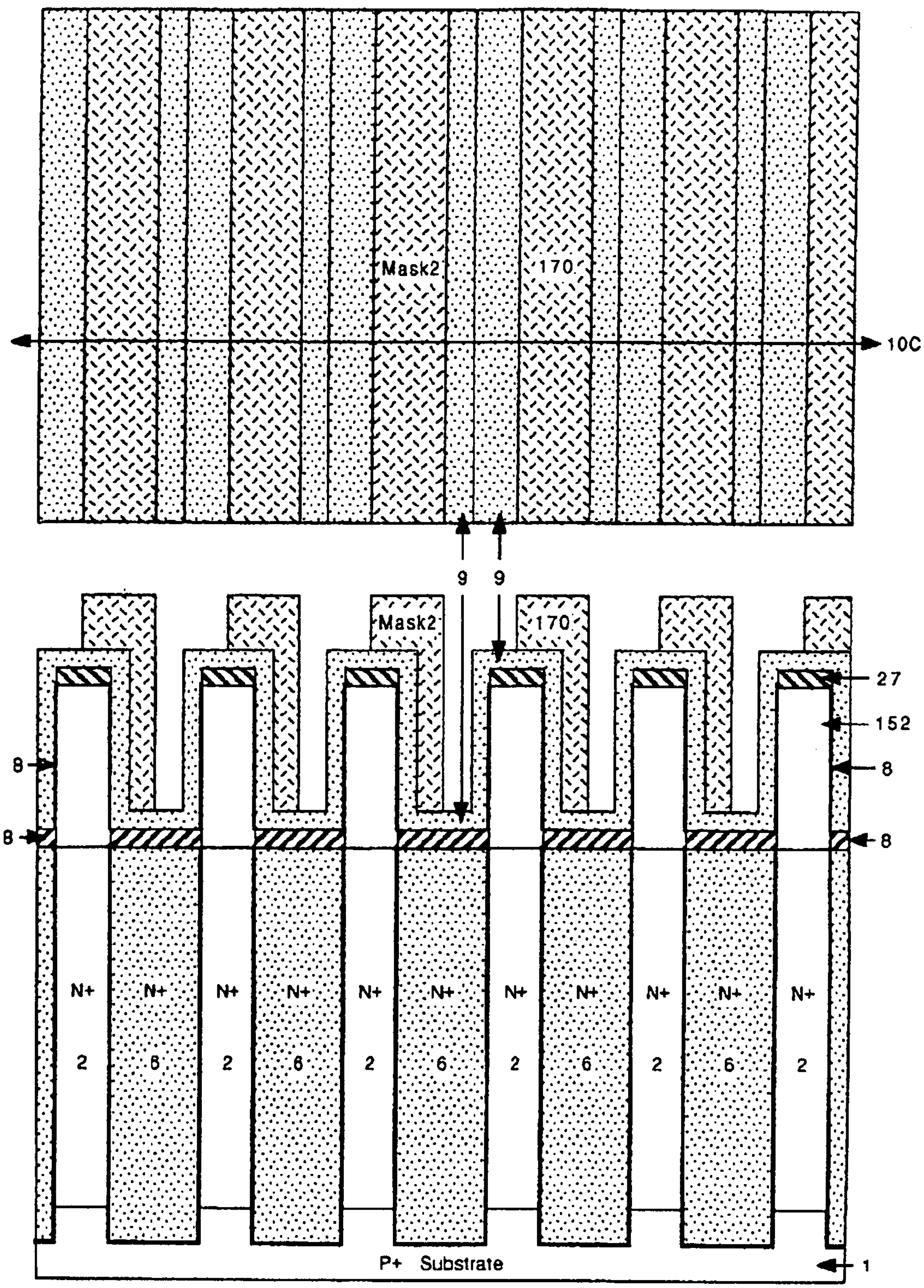

Mask2
170
10C
9
9
Mask2
170
27
152
8
8
8
8
N+
2
N+
6
N+
2
N+
6
N+
2
N+
6
N+
2
N+
6
N+
2
N+
6
N+
2
P+ Substrate
1

Fig.10C

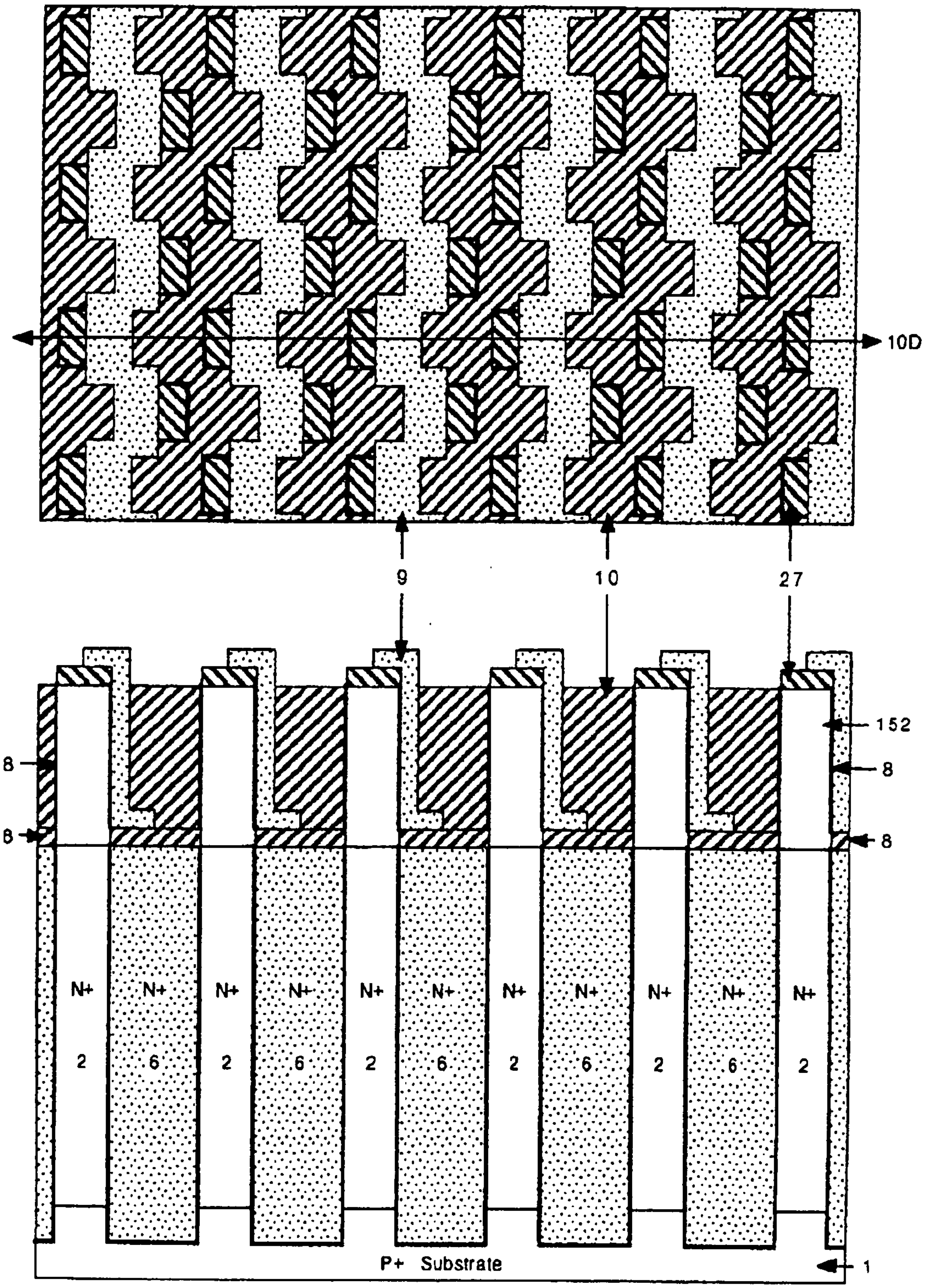


Fig.10D

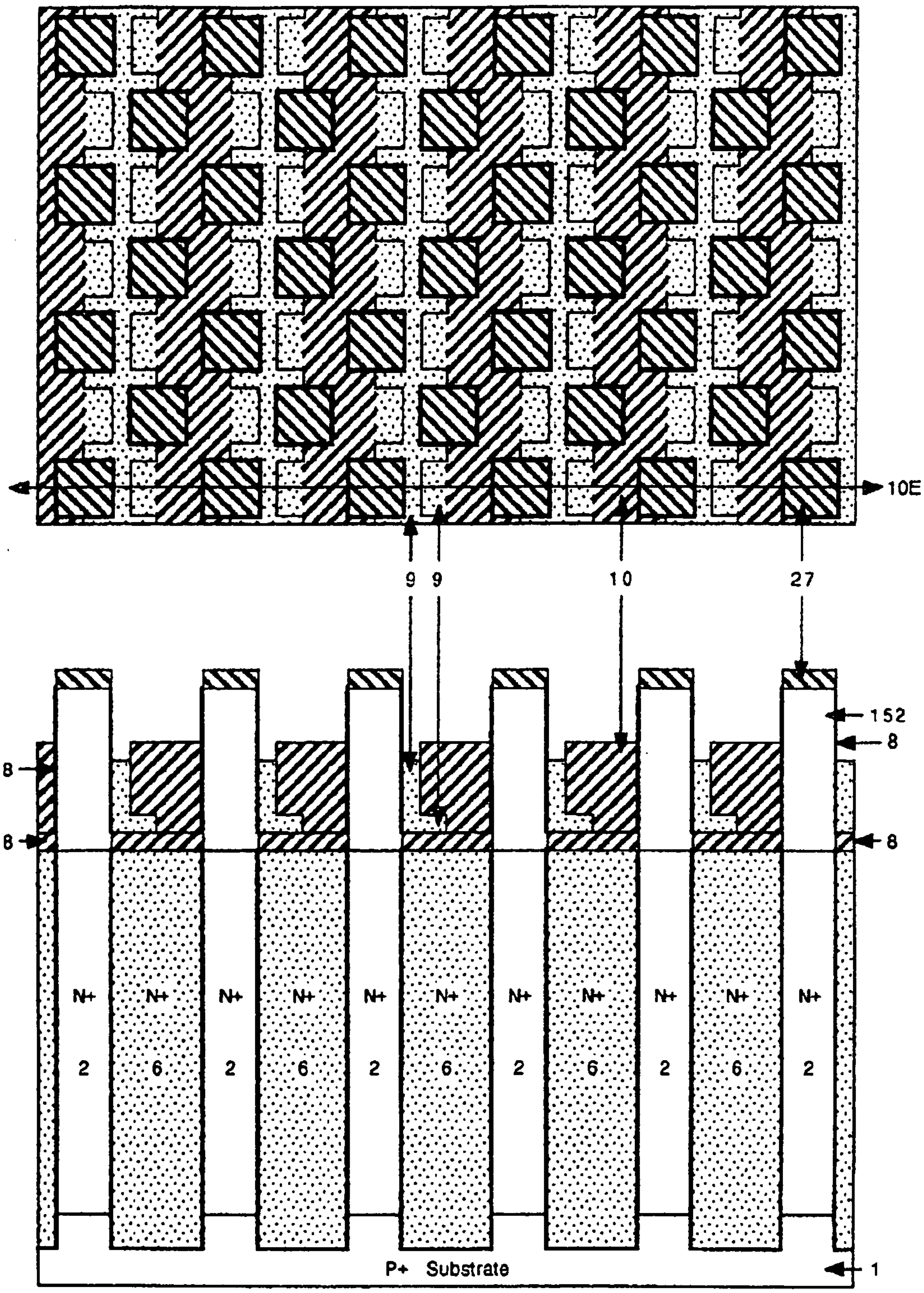


Fig.10E

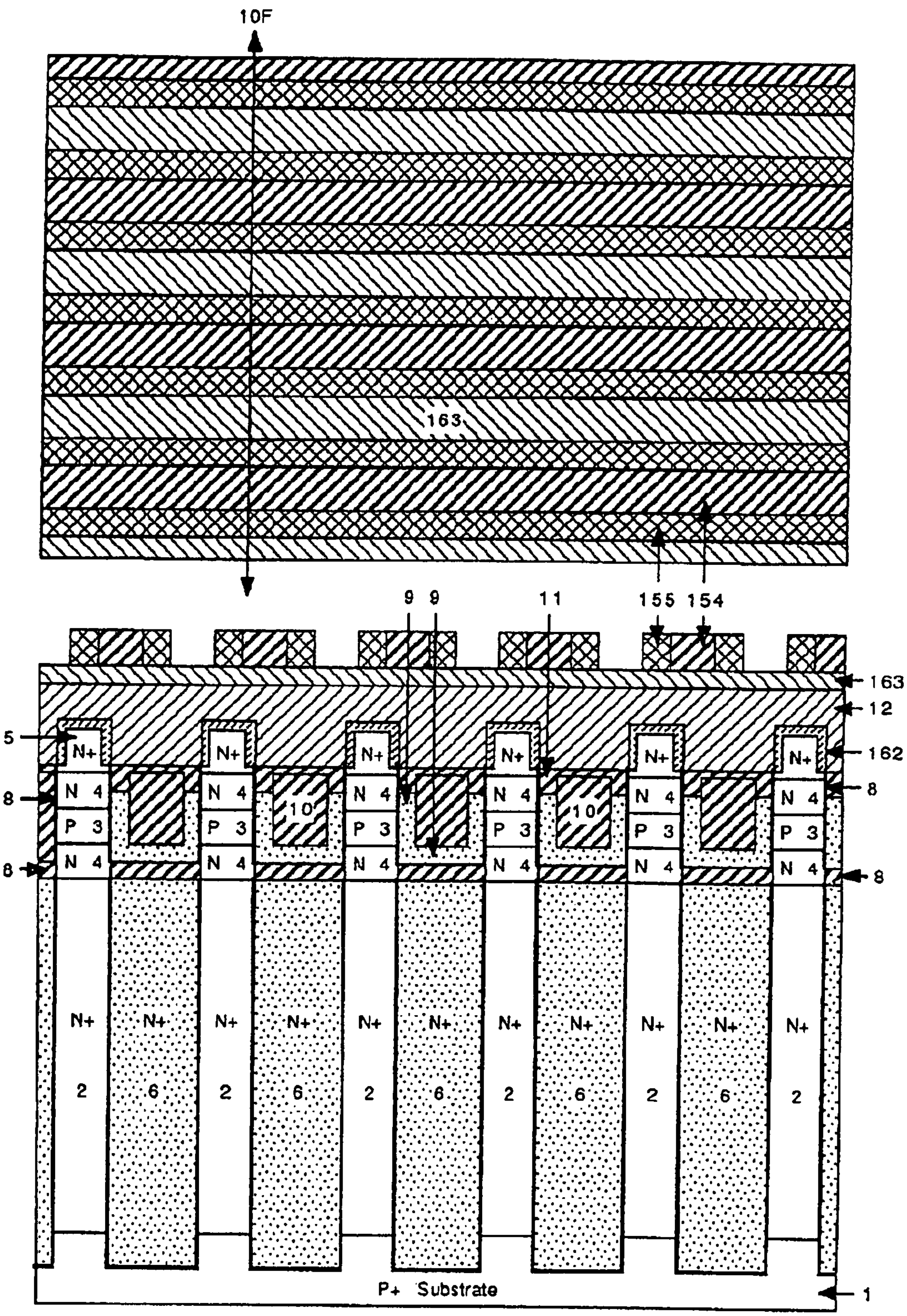
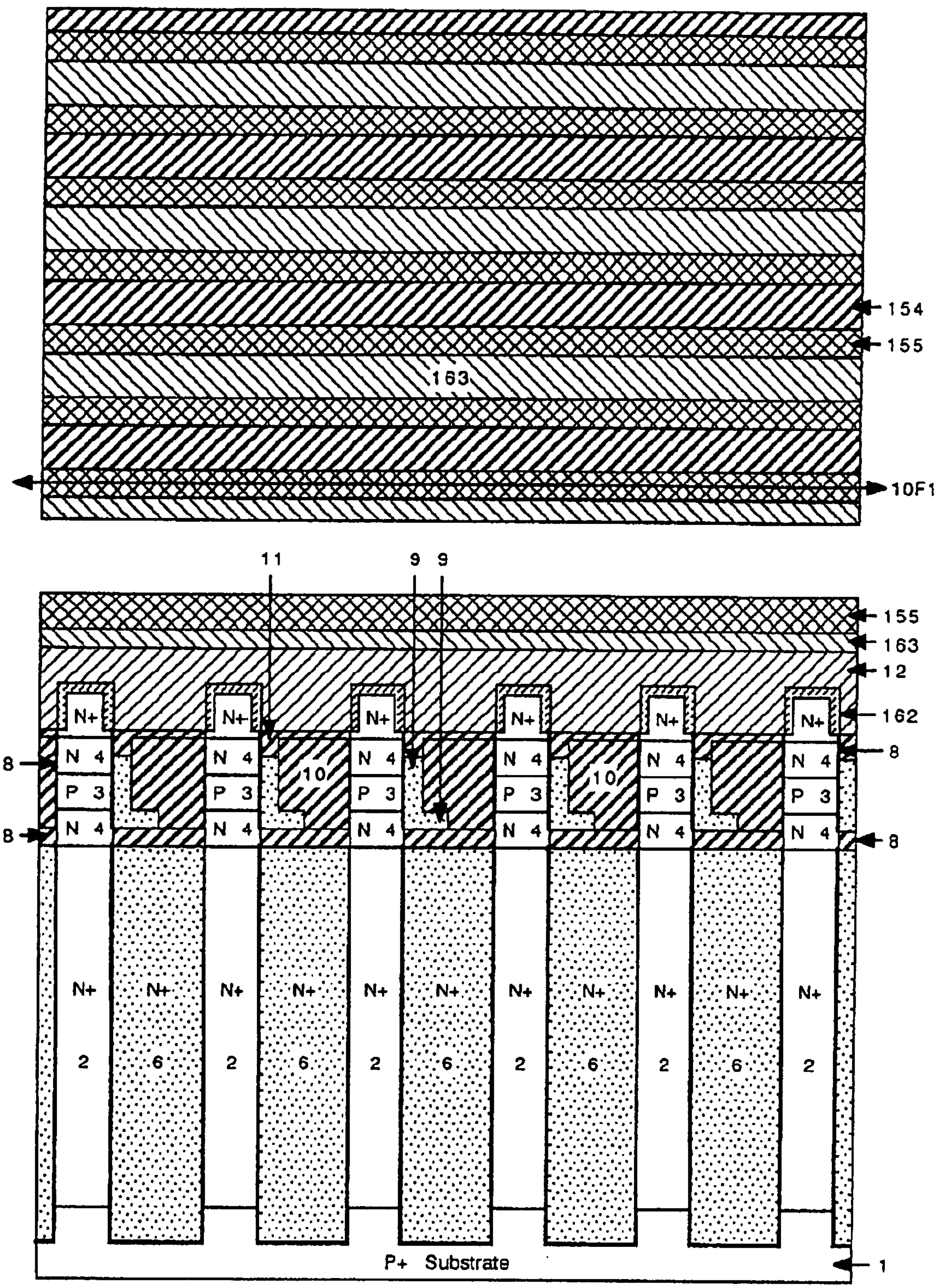


Fig.10F



154
155
163
10F1
11
9
9
155
163
12
162
8
N+
N 4
P 3
10
N+
2
6
P+ Substrate
1

Fig.10F1

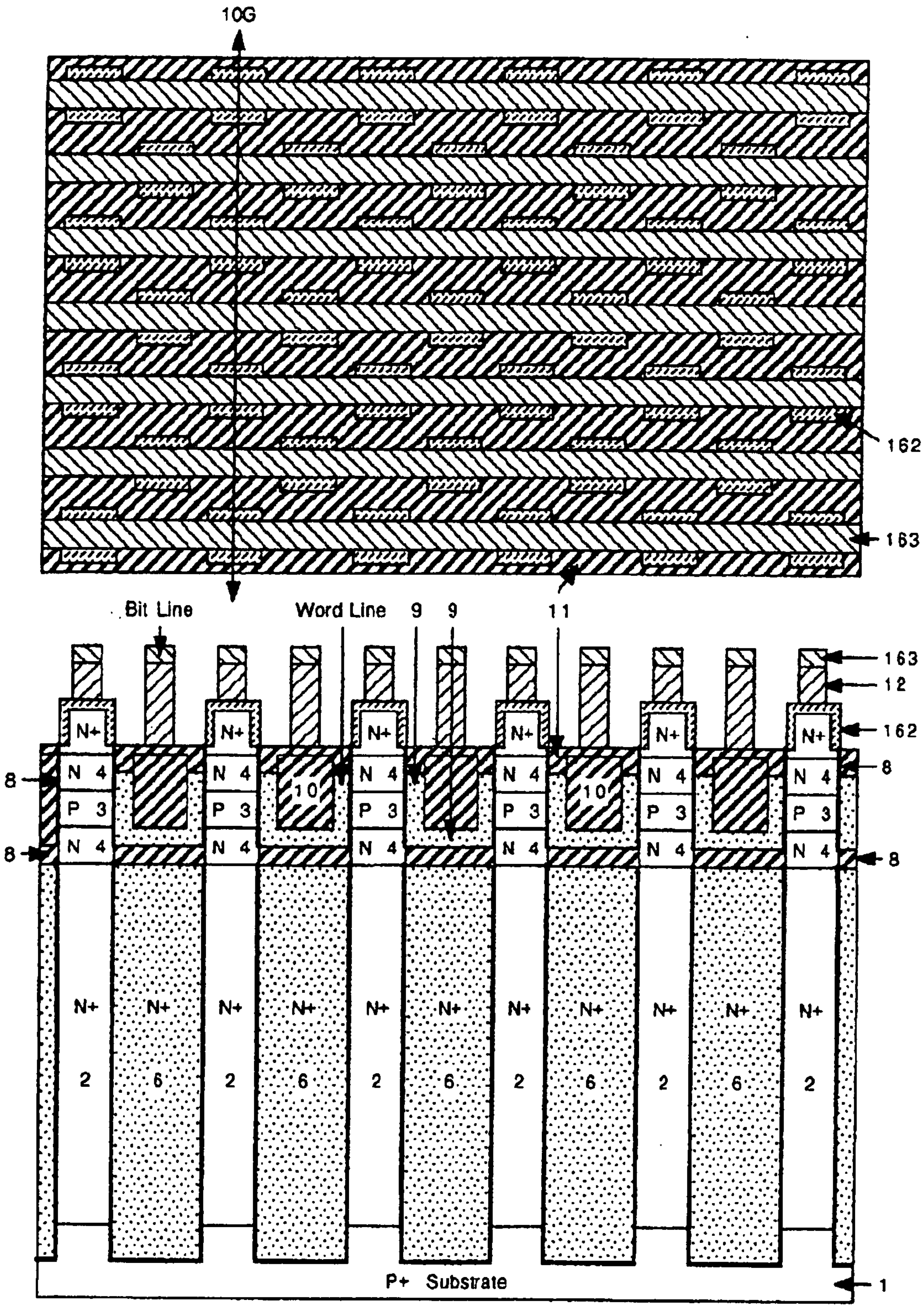

10G
162
163
Bit Line
Word Line
9
9
11
163
12
162
8
8
8
8
N+
N 4
P 3
N 4
10
N+
2
6
P+ Substrate
1

Fig.10G

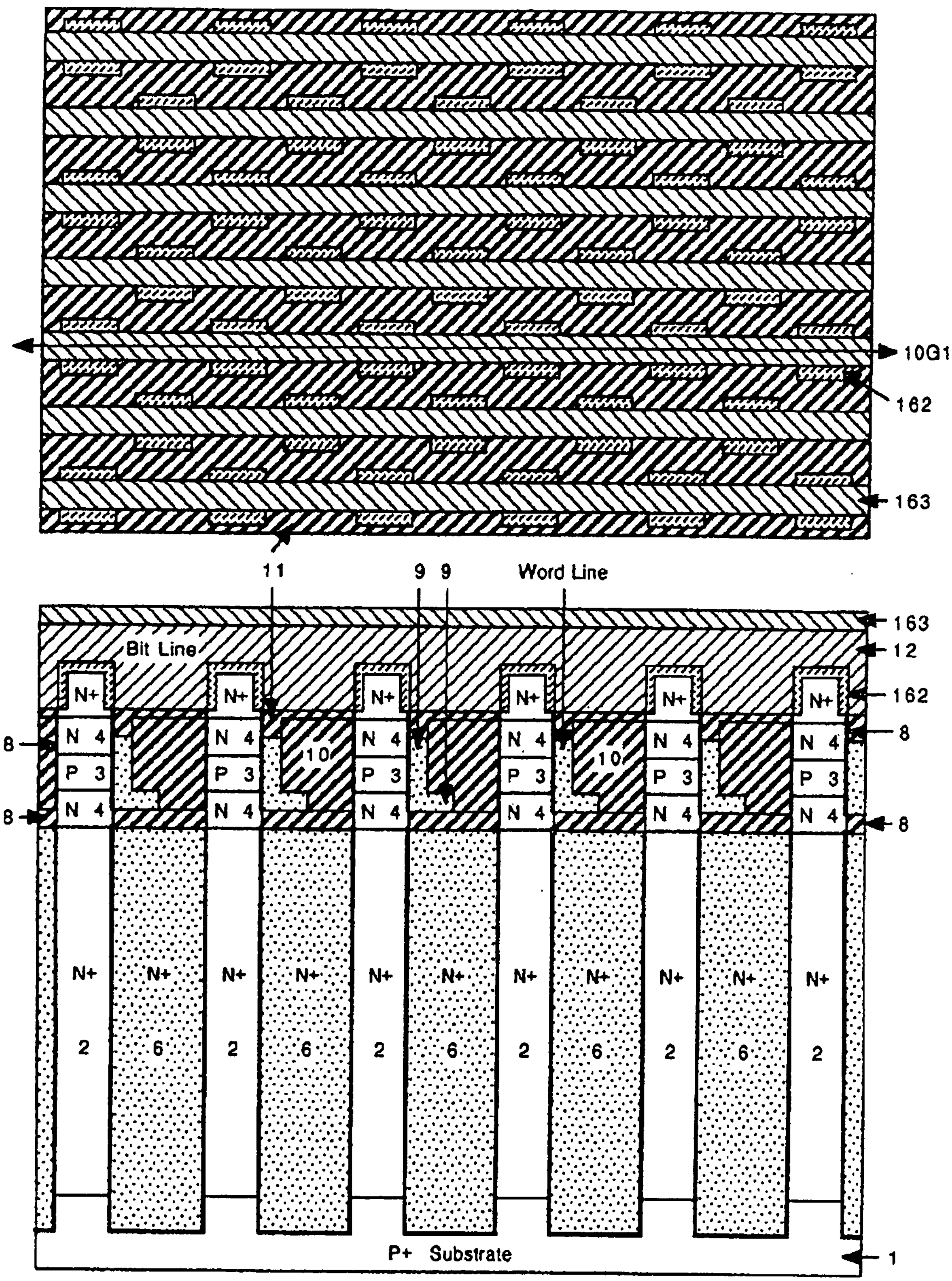
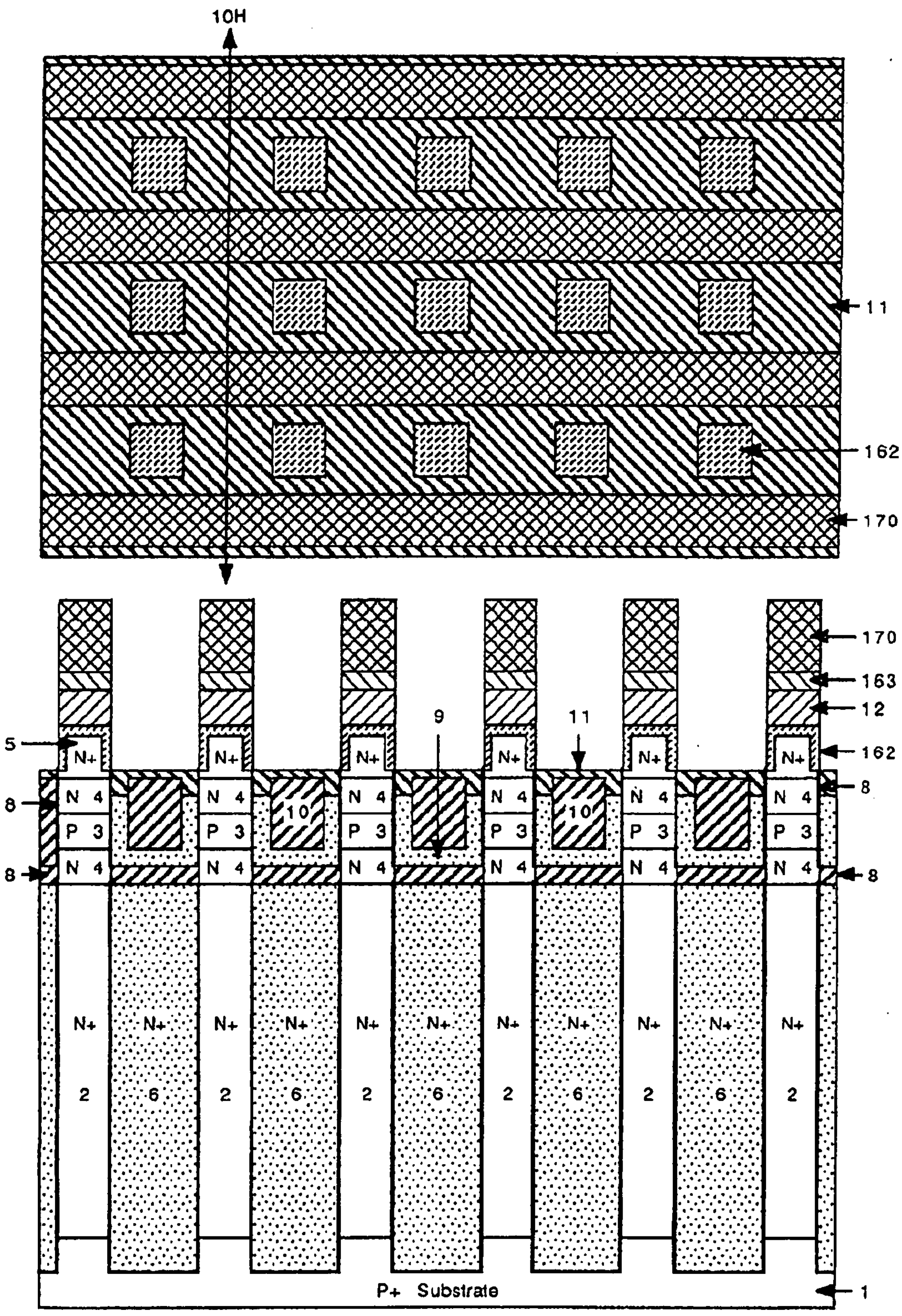
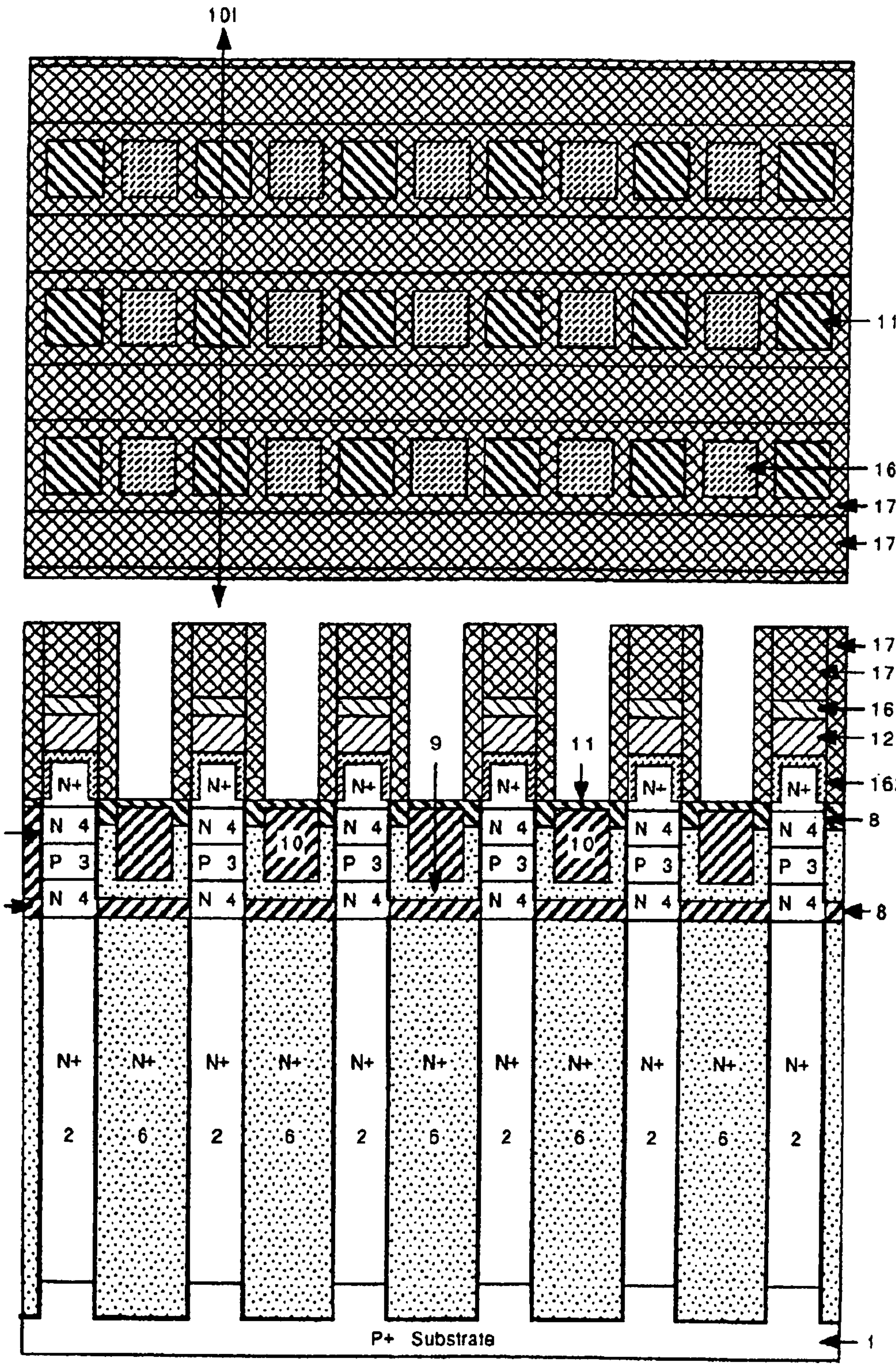

10G1
162
163
11
9
9
Word Line
163
12
162
8
Bit Line
N+
N 4
P 3
10
8
N+
2
6
P+ Substrate
1

Fig.10G1



10H
11
162
170
170
163
12
162
8
5
N+
N 4
P 3
N 4
10
9
11
N+
2
6
P+ Substrate
1

Fig.10H



101
11
162
171
170
171
170
163
12
9
11
162
8
N+
N 4
P 3
N 4
10
8
N+
2
6
P+ Substrate
1

Fig.10I

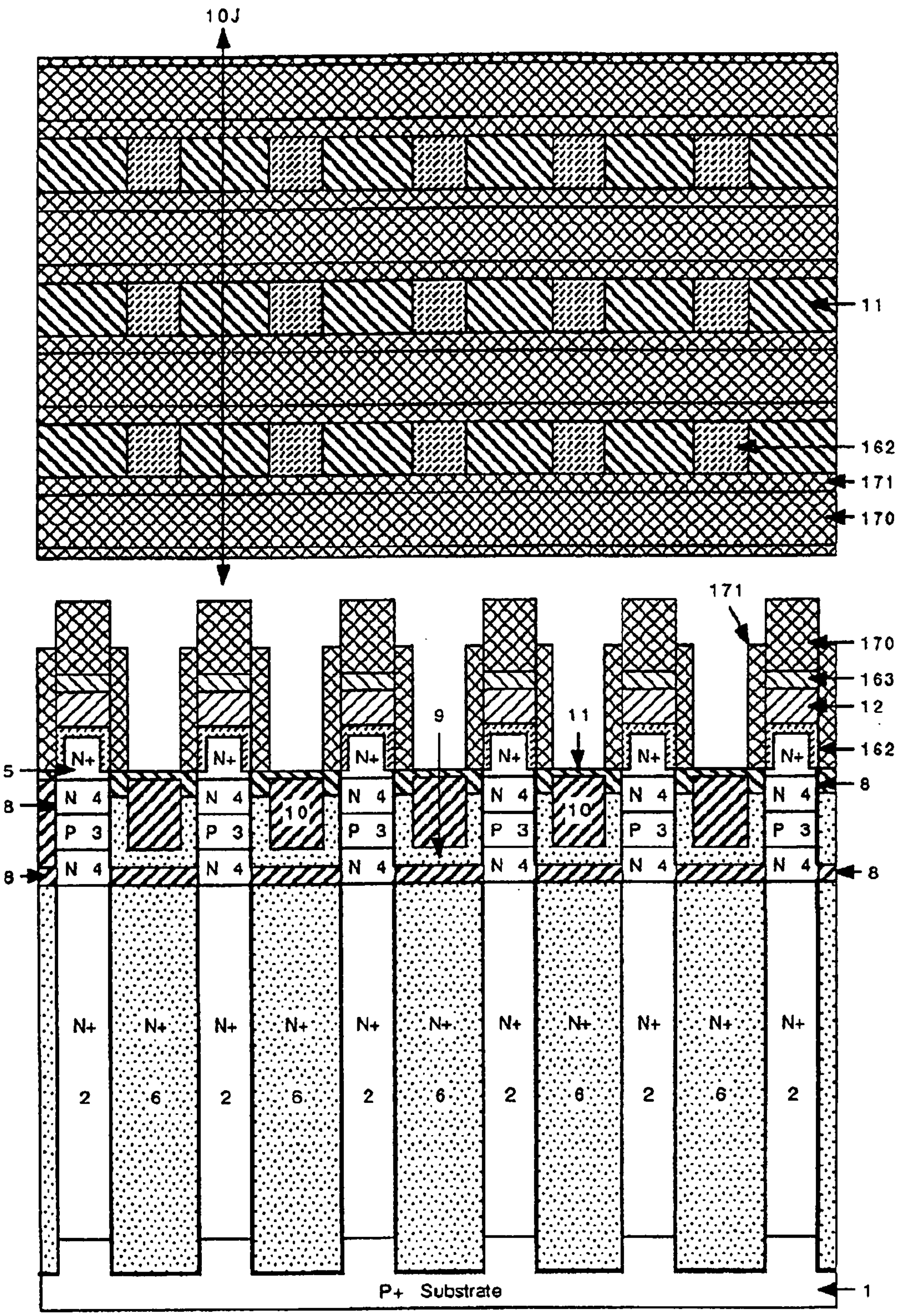

10J
11
162
171
170
171
170
163
12
162
9
11
5
8
8
8
8
N+
N 4
P 3
10
N+
2
6
P+ Substrate
1

Fig.10J

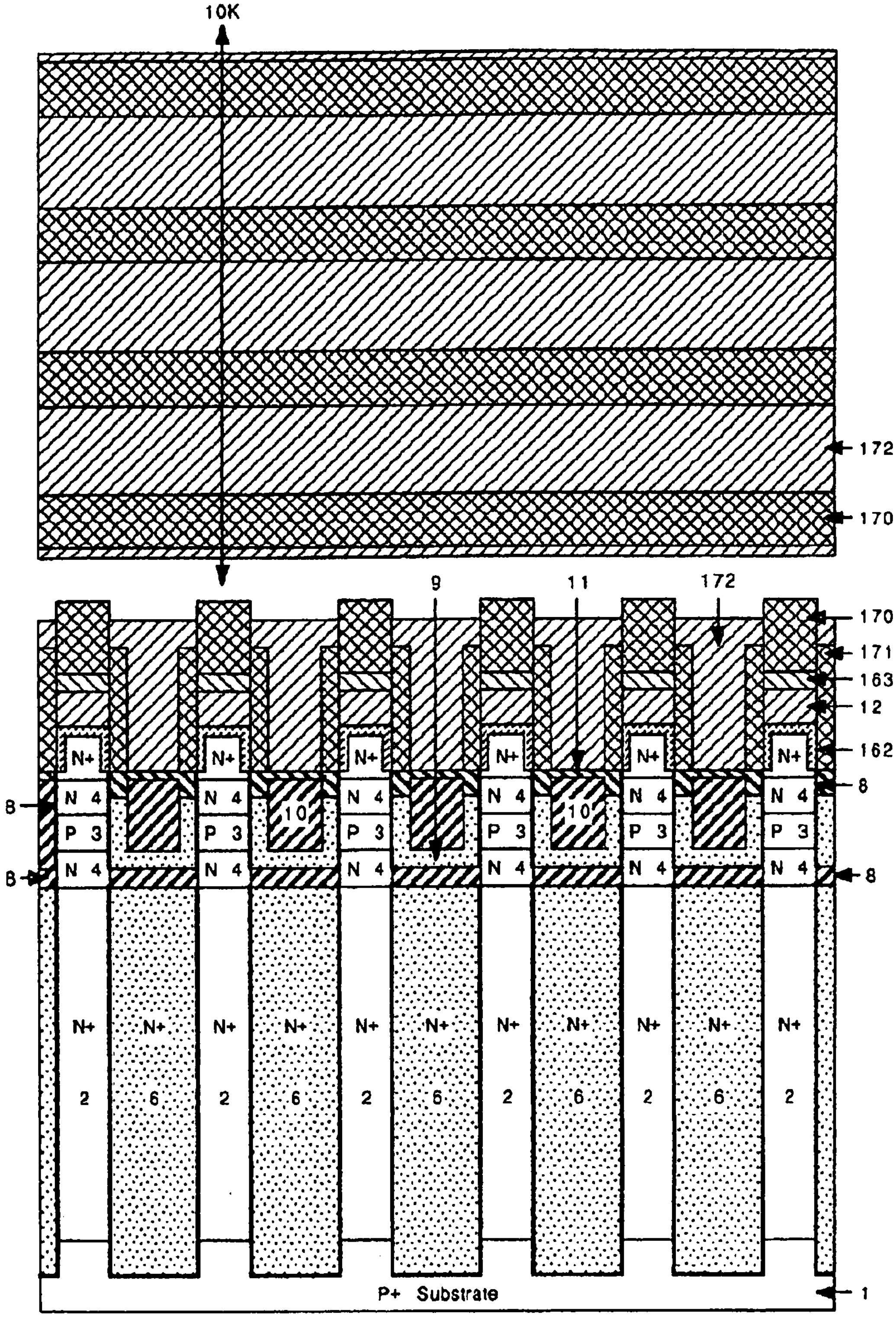

10K
172
170
9
11
172
170
171
163
12
162
8
N+
N 4
P 3
10
P+ Substrate
2
6
1

Fig.10K

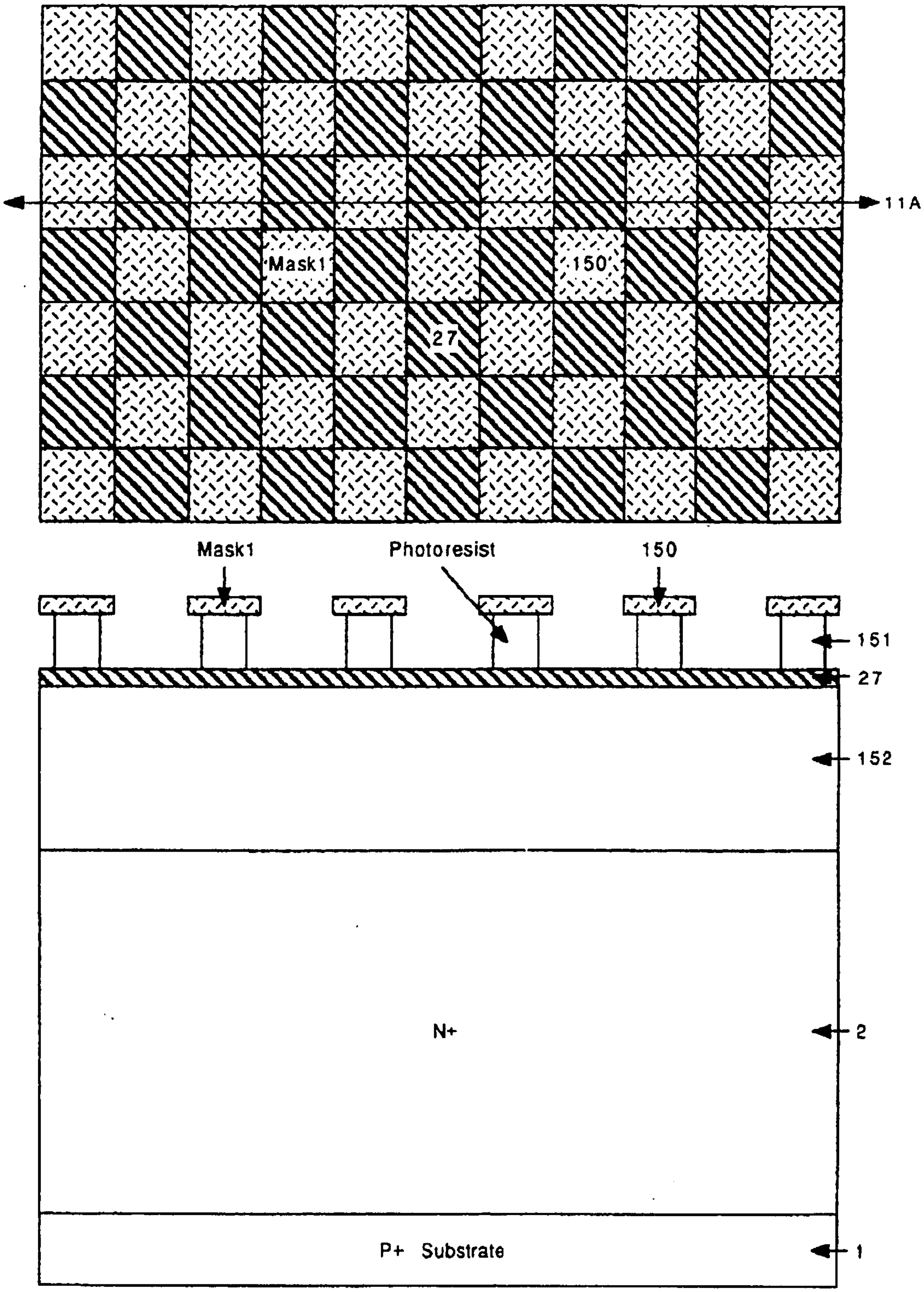

11A
Mask1
150
27
Mask1
Photoresist
150
151
27
152
N+
2
P+ Substrate
1

Fig.11A

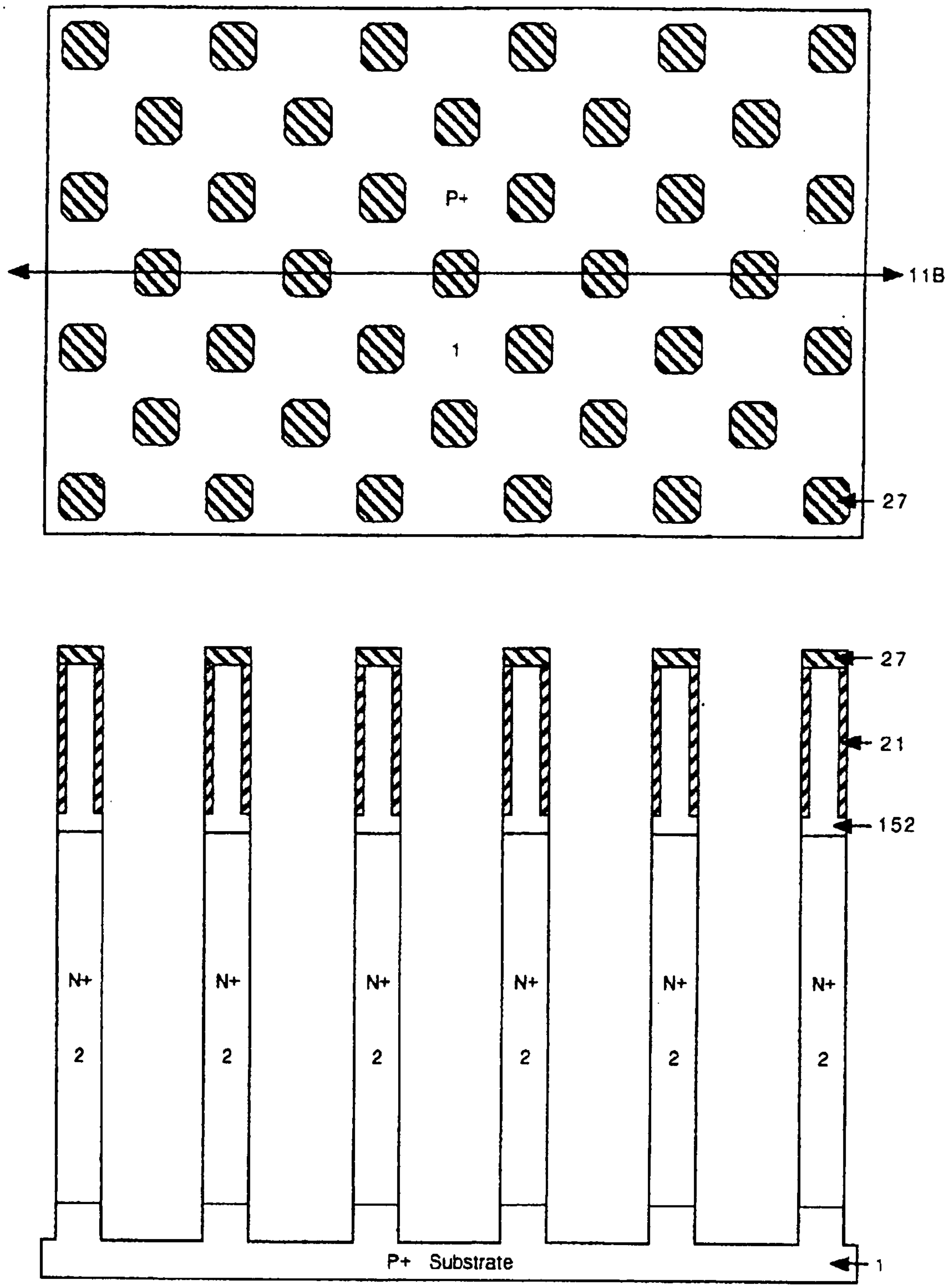
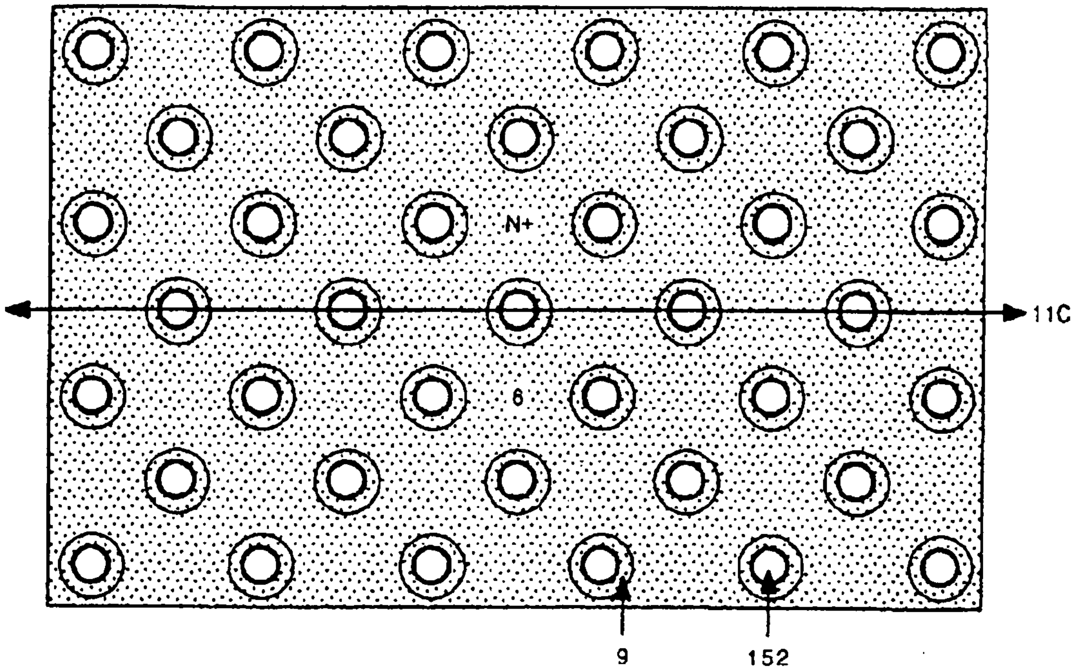


Fig.11B



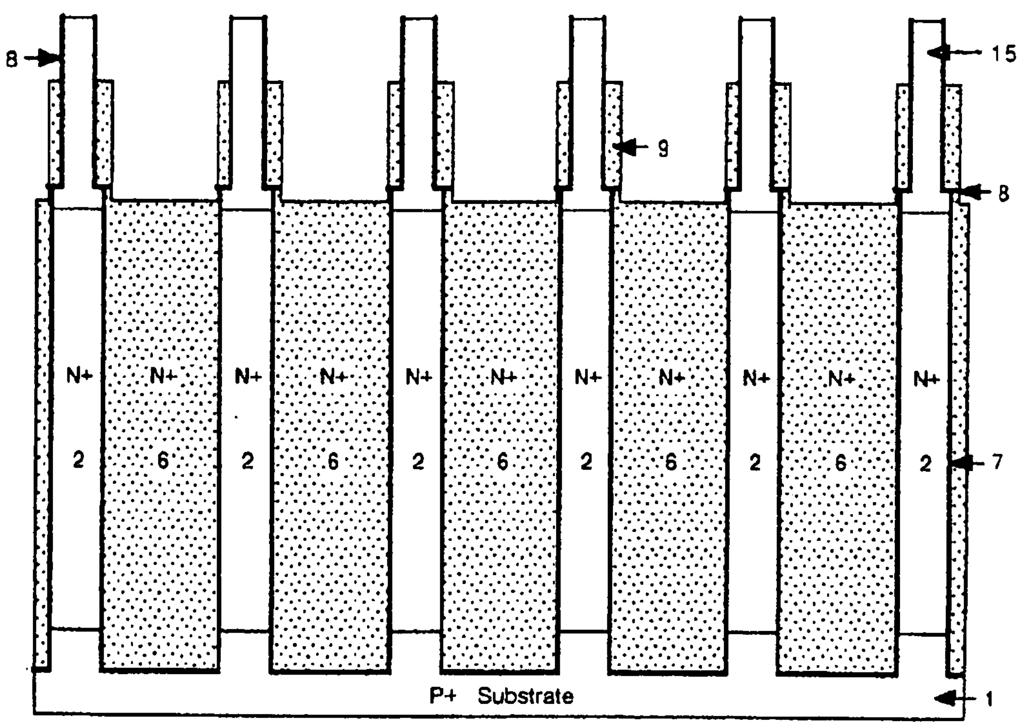


Fig.11C

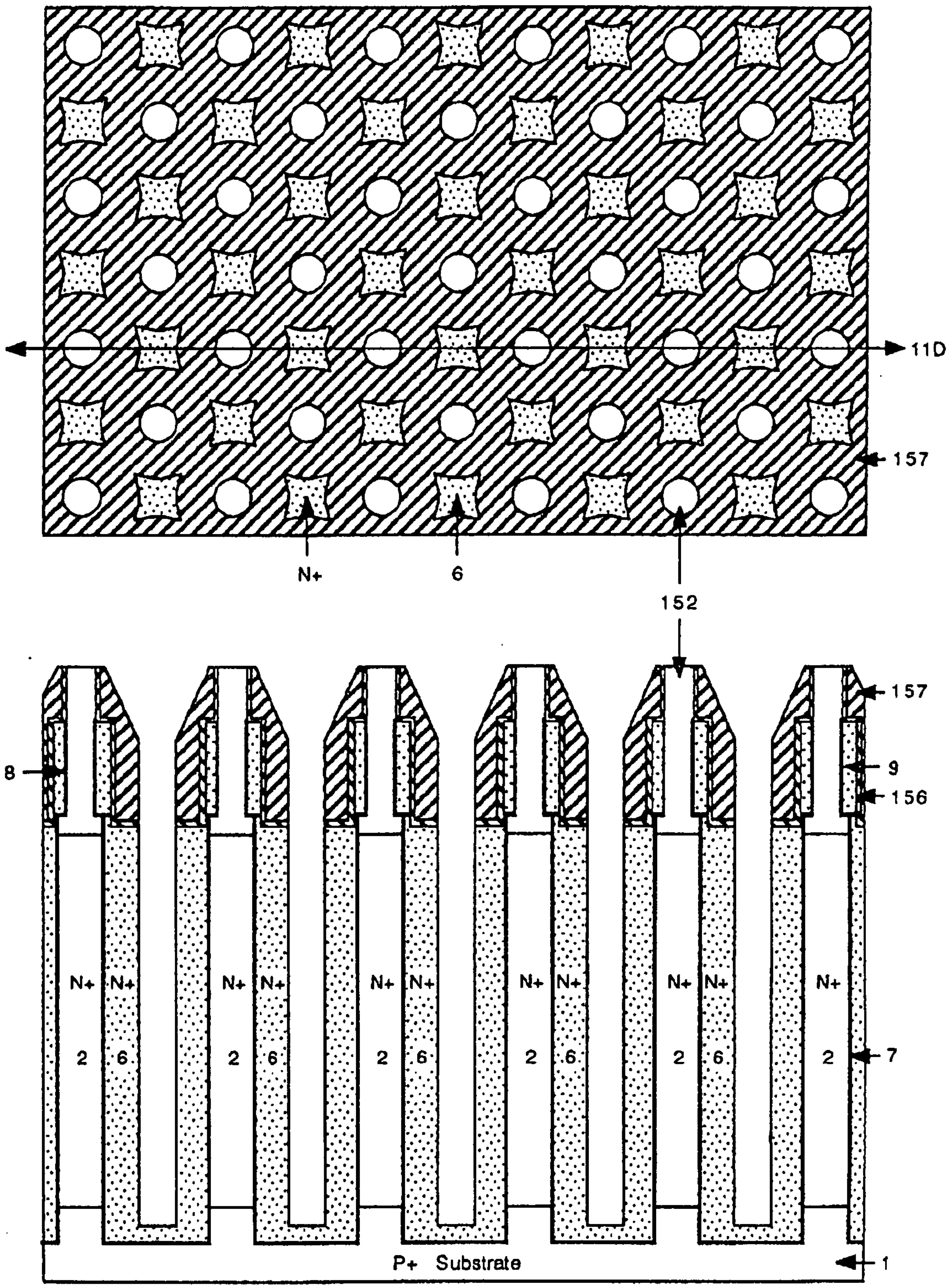


Fig.11D

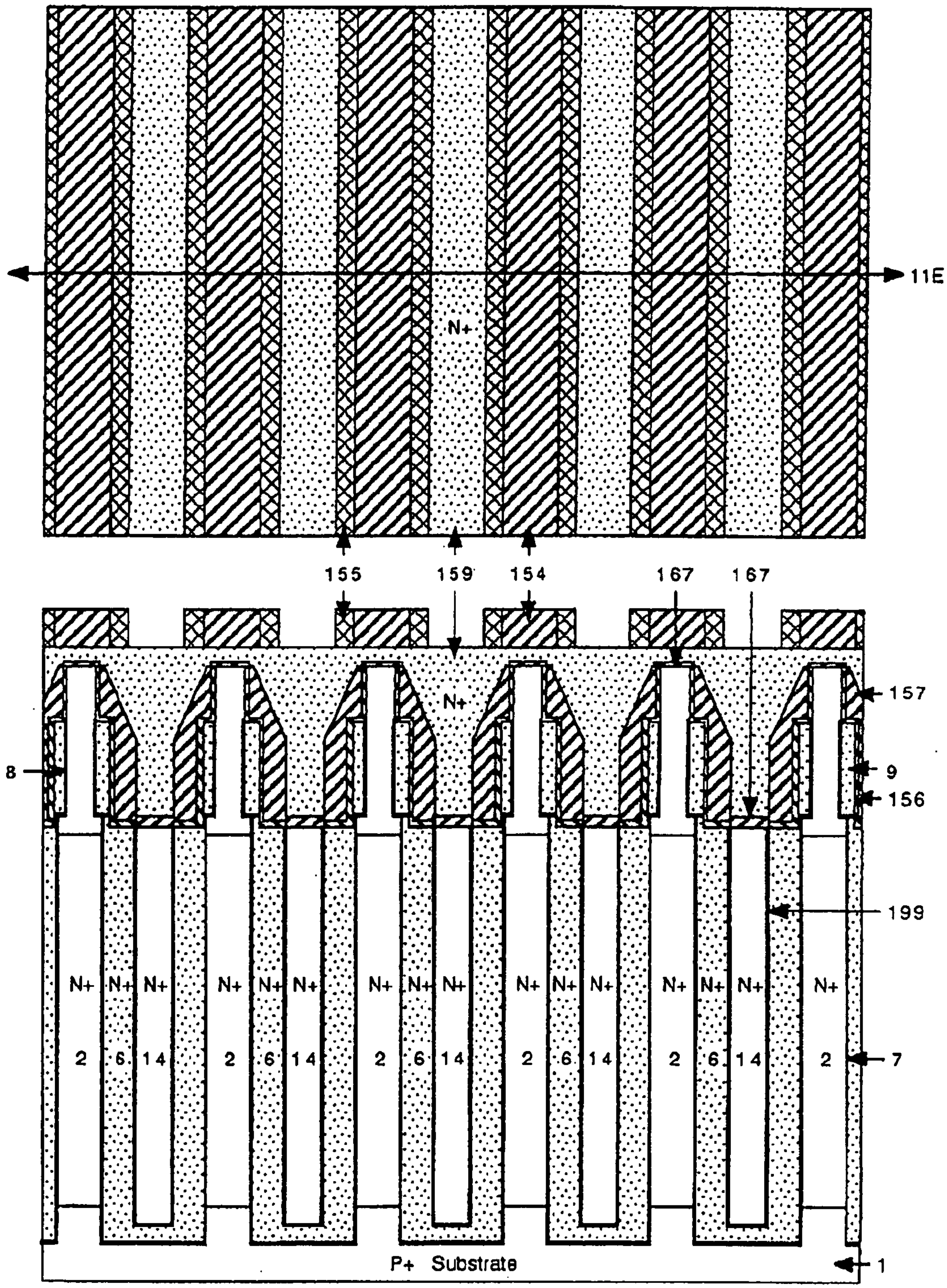


Fig.11E

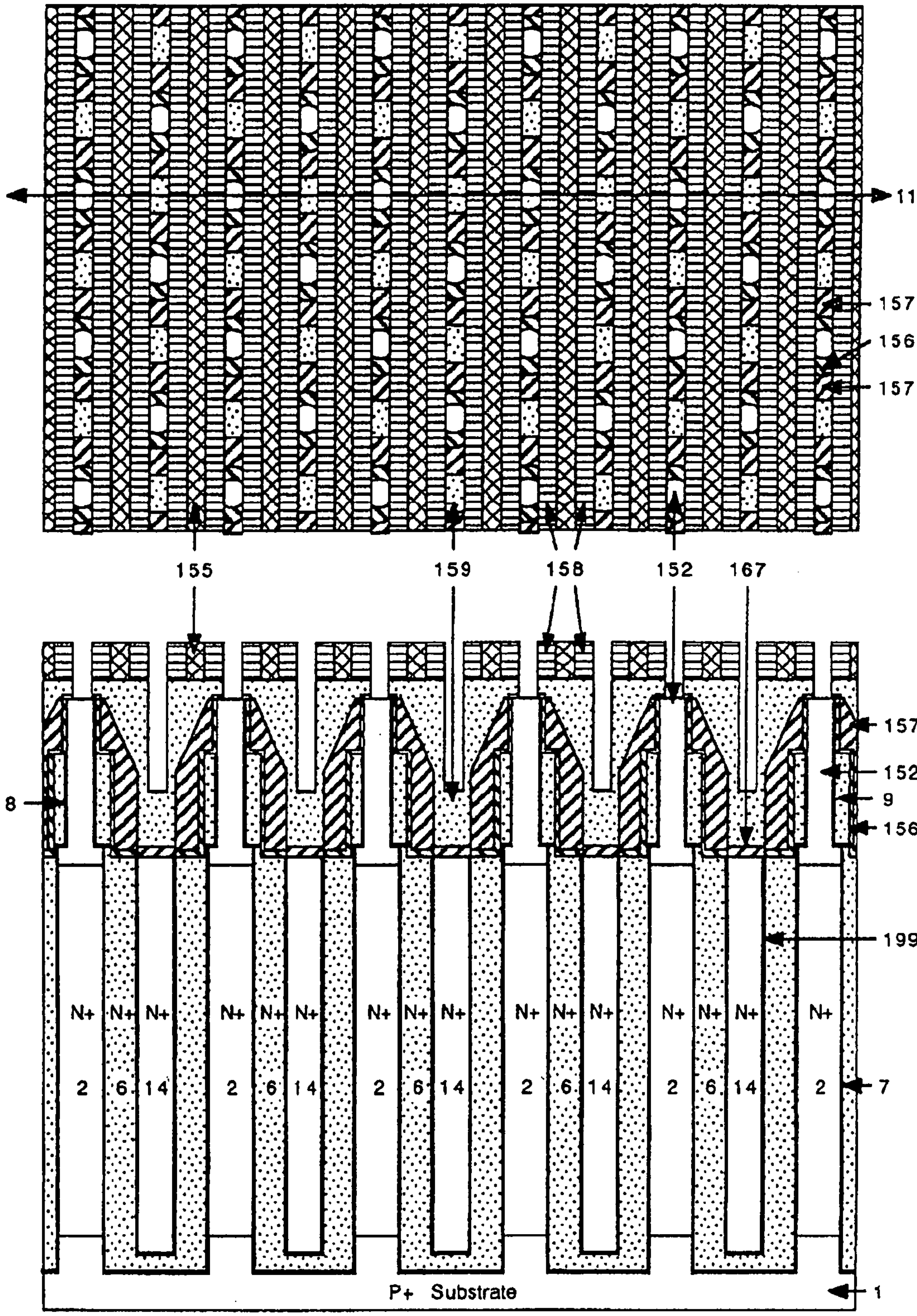

11F
157
156
157
155
159
158
152
167
157
152
9
156
8
199
N+
N+
N+
2
6
14
7
P+ Substrate
1

Fig.11F

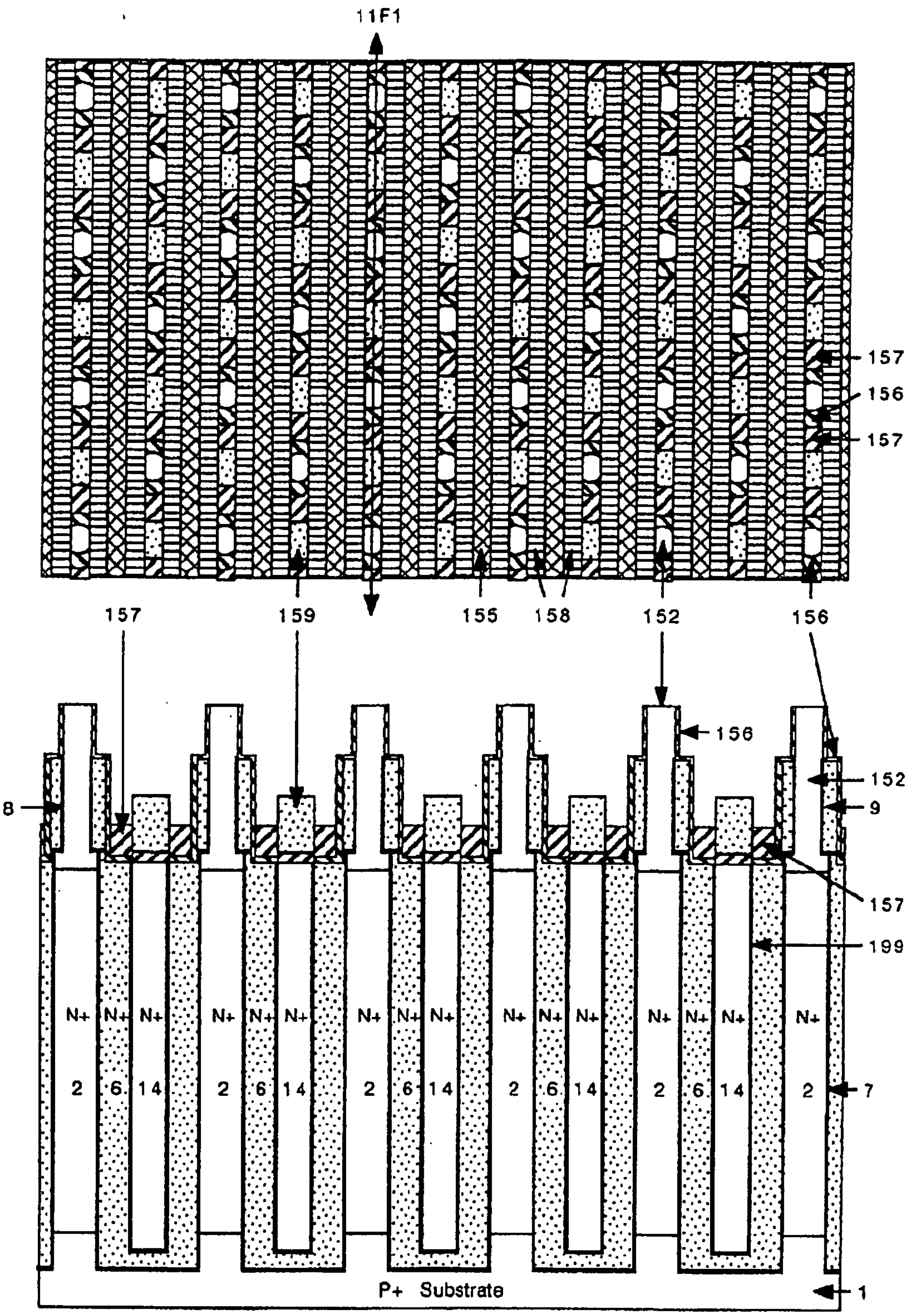

11F1
157
156
157
157
159
155
158
152
156
156
152
9
8
157
199
N+
2
6
14
7
P+ Substrate
1

Fig.11F1

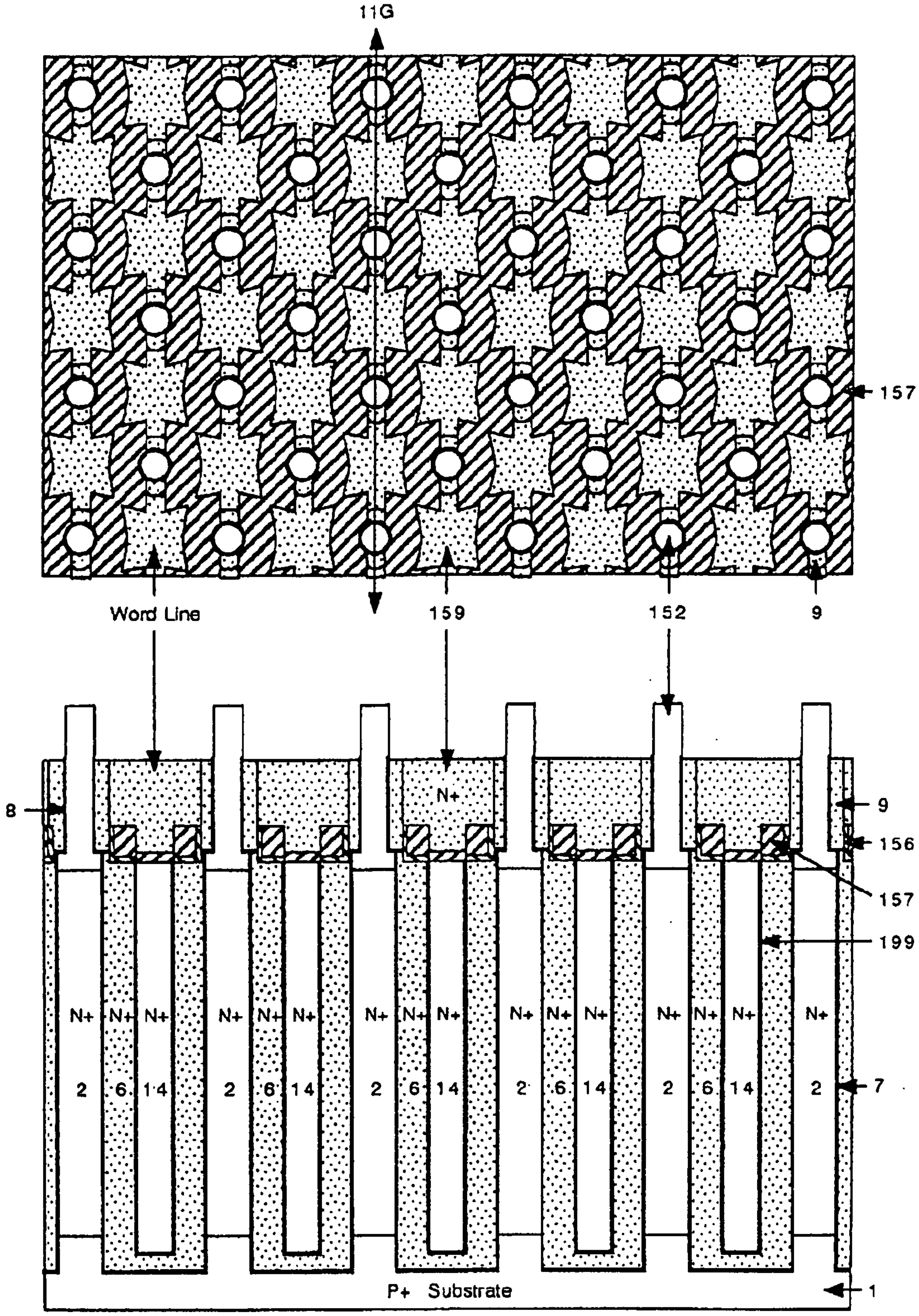

11G
157
Word Line
159
152
9
8
N+
9
156
157
199
N+
N+
N+
2
6
14
7
P+ Substrate
1

Fig.11G

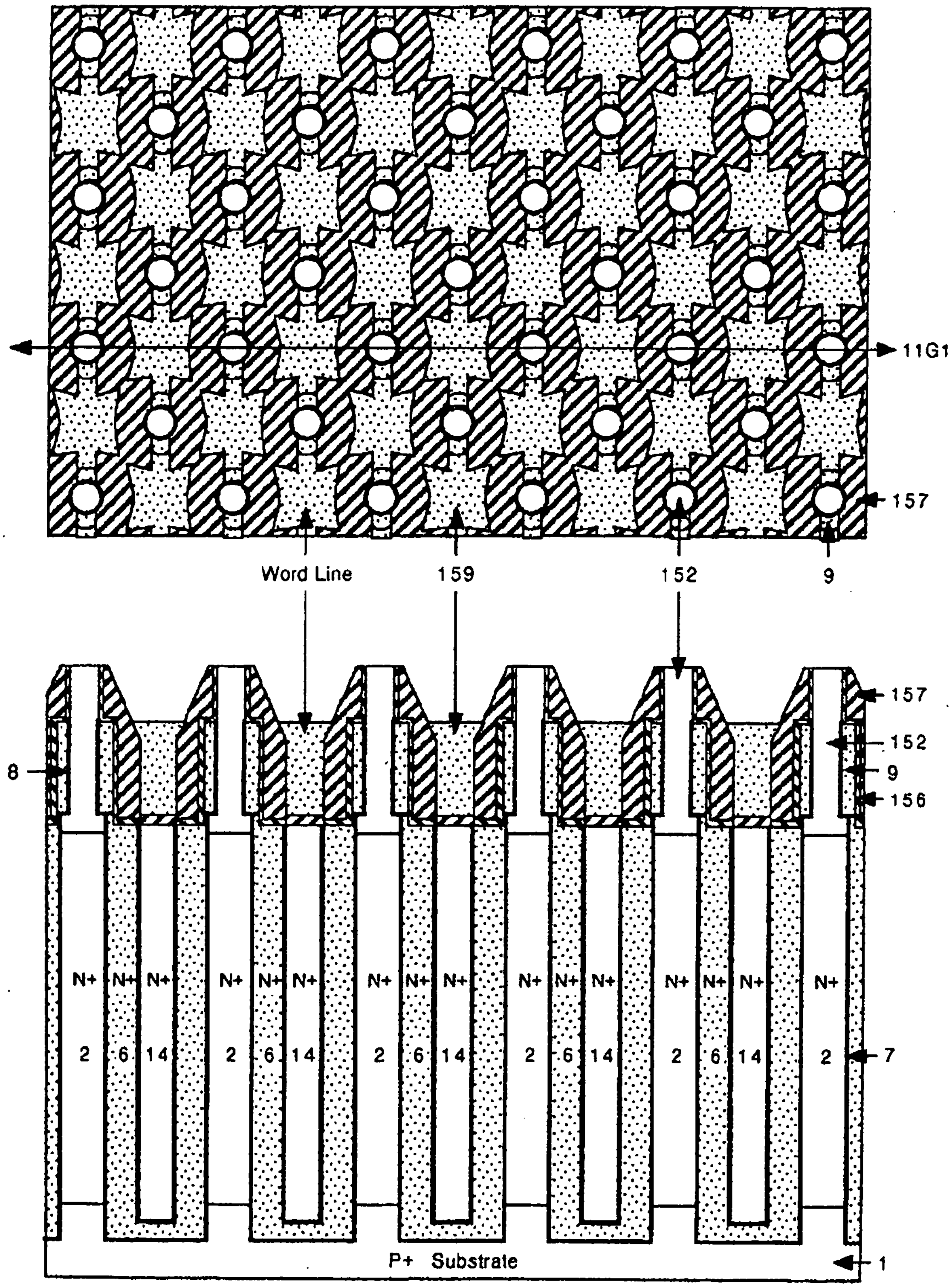

11G1
157
Word Line
159
152
9
157
152
8
9
156
N+
2
6
14
7
P+ Substrate
1

Fig.11G1

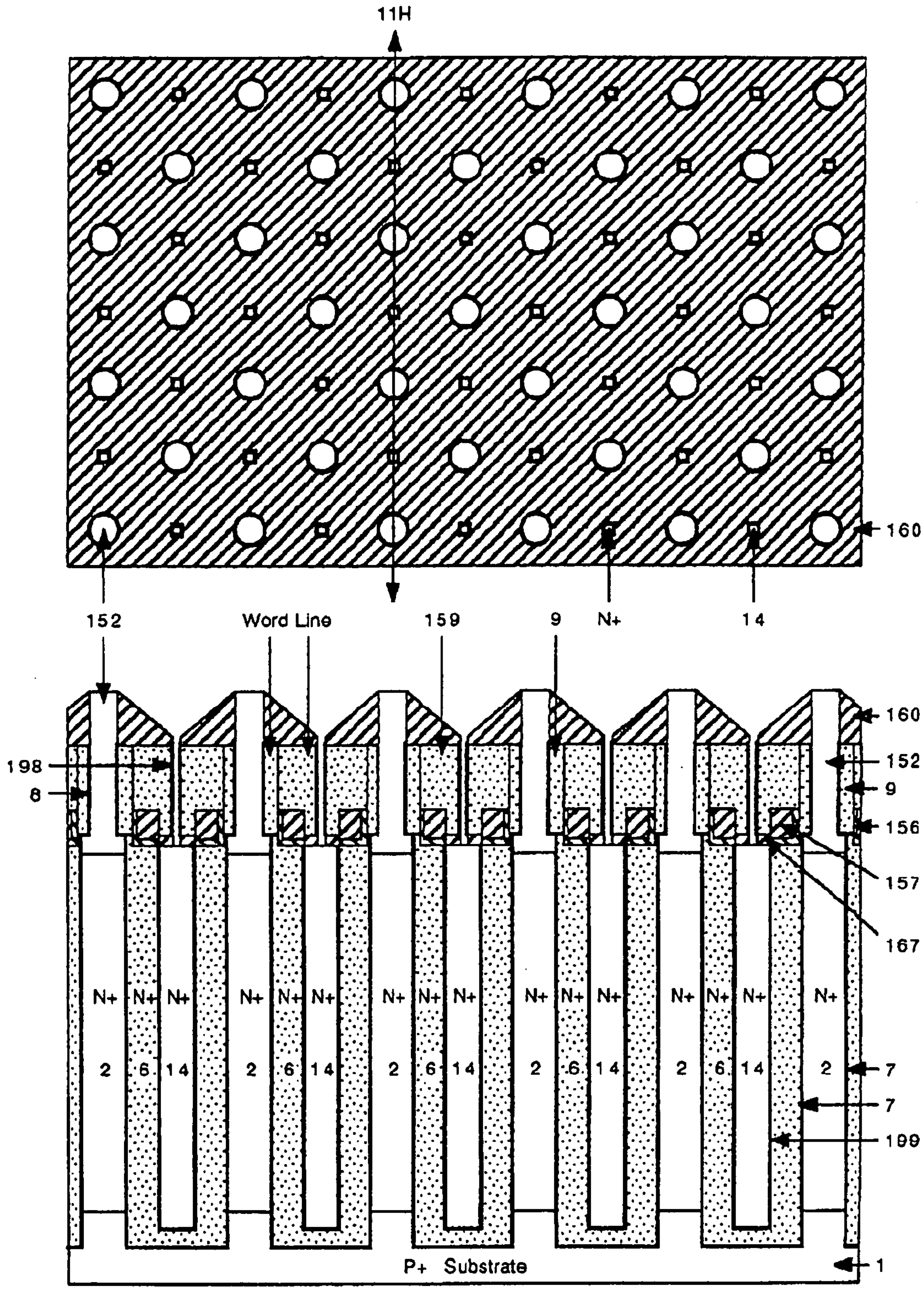
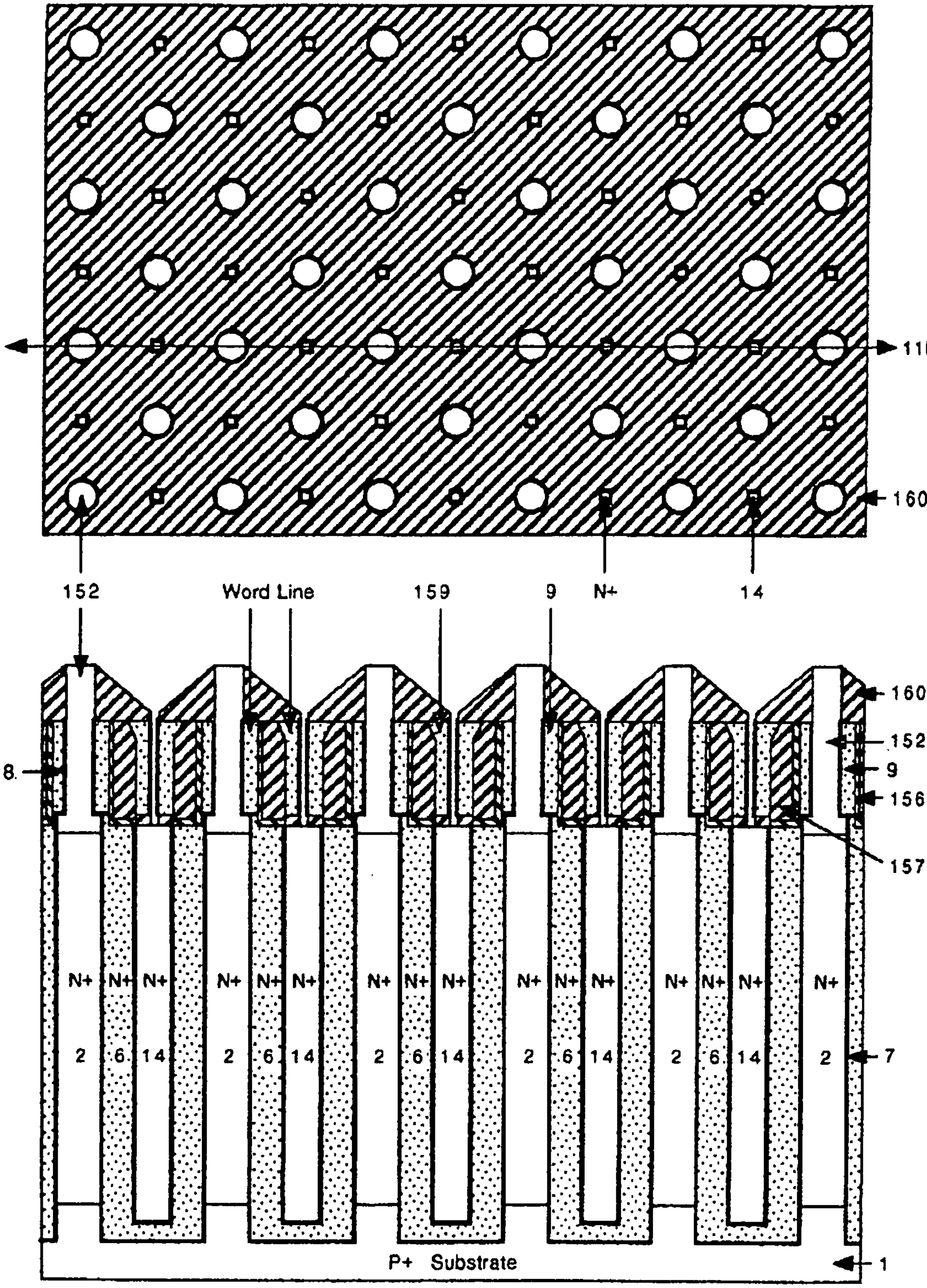

11H
160
152
Word Line
159
9
N+
14
198
8
152
9
156
157
167
N+
2
6
14
7
199
P+ Substrate
1

Fig.11H



11H1
160
152
Word Line
159
9
N+
14
160
152
8
9
156
157
N+
2
6
14
7
P+ Substrate
1

Fig.11H1

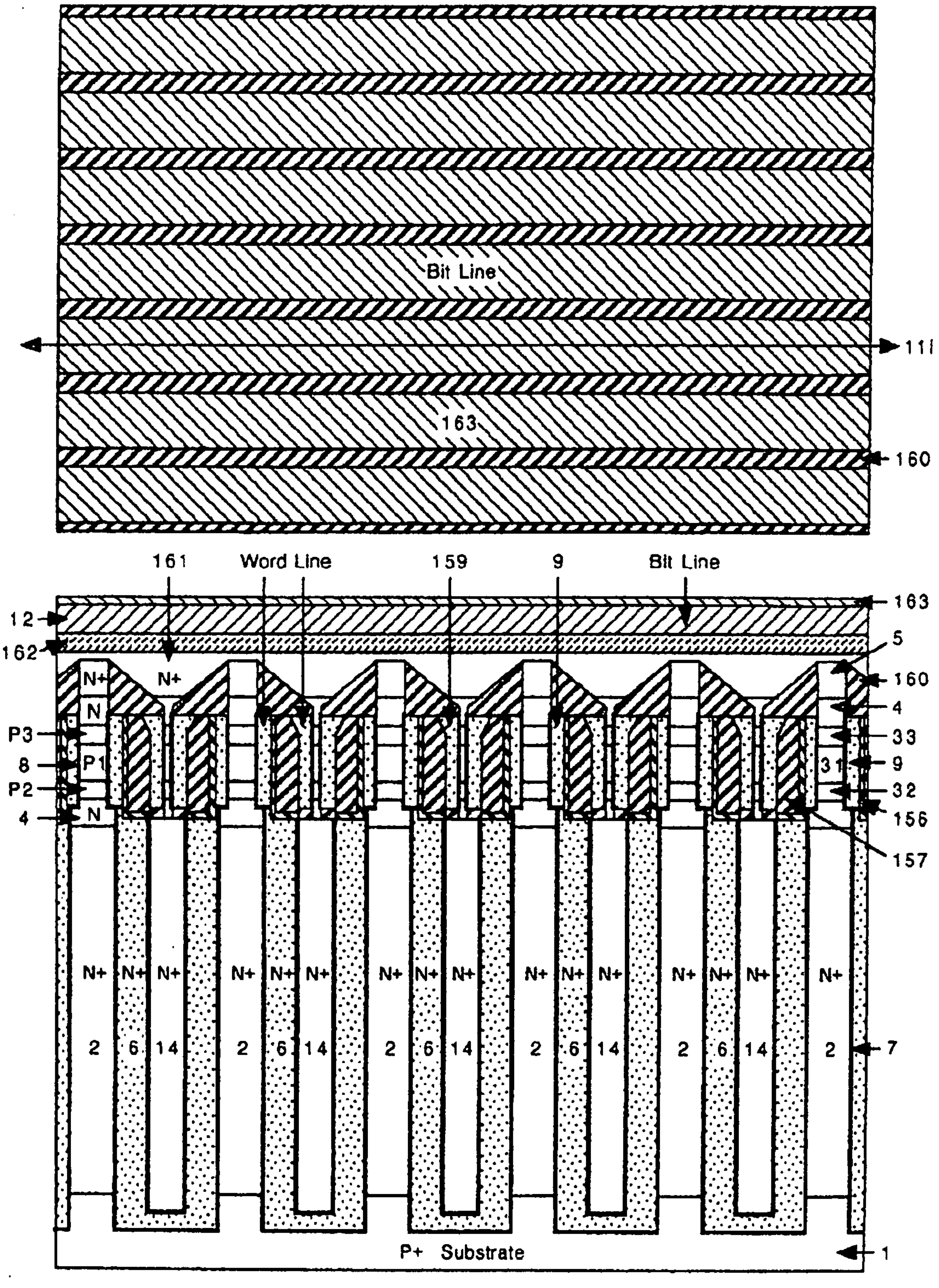
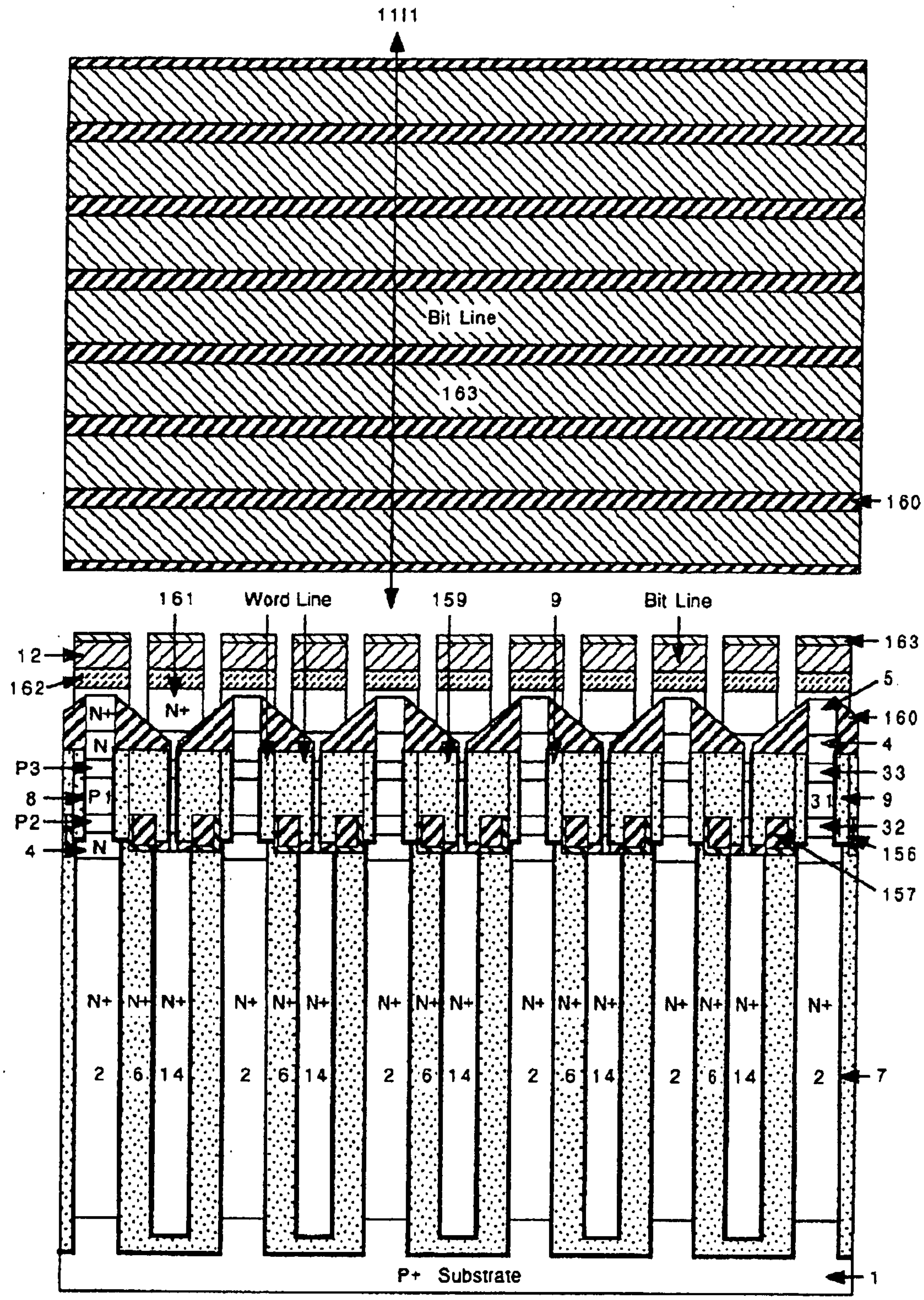

Bit Line
111
163
160
161
Word Line
159
9
Bit Line
163
12
162
5
160
4
33
9
32
156
157
N+
N
P3
8
P1
P2
4
31
N+
2
6
14
7
P+ Substrate
1

Fig.11I



1111
Bit Line
163
160
161
Word Line
159
9
Bit Line
163
12
162
N+
N+
5
160
N
4
P3
33
8
P1
31
9
P2
32
4
N
156
157
N+
N+
N+
N+
N+
N+
N+
N+
N+
N+
N+
N+
N+
N+
N+
N+
2
6
14
2
6
14
2
6
14
2
6
14
2
6
14
2
7
P+ Substrate
1

Fig.1111

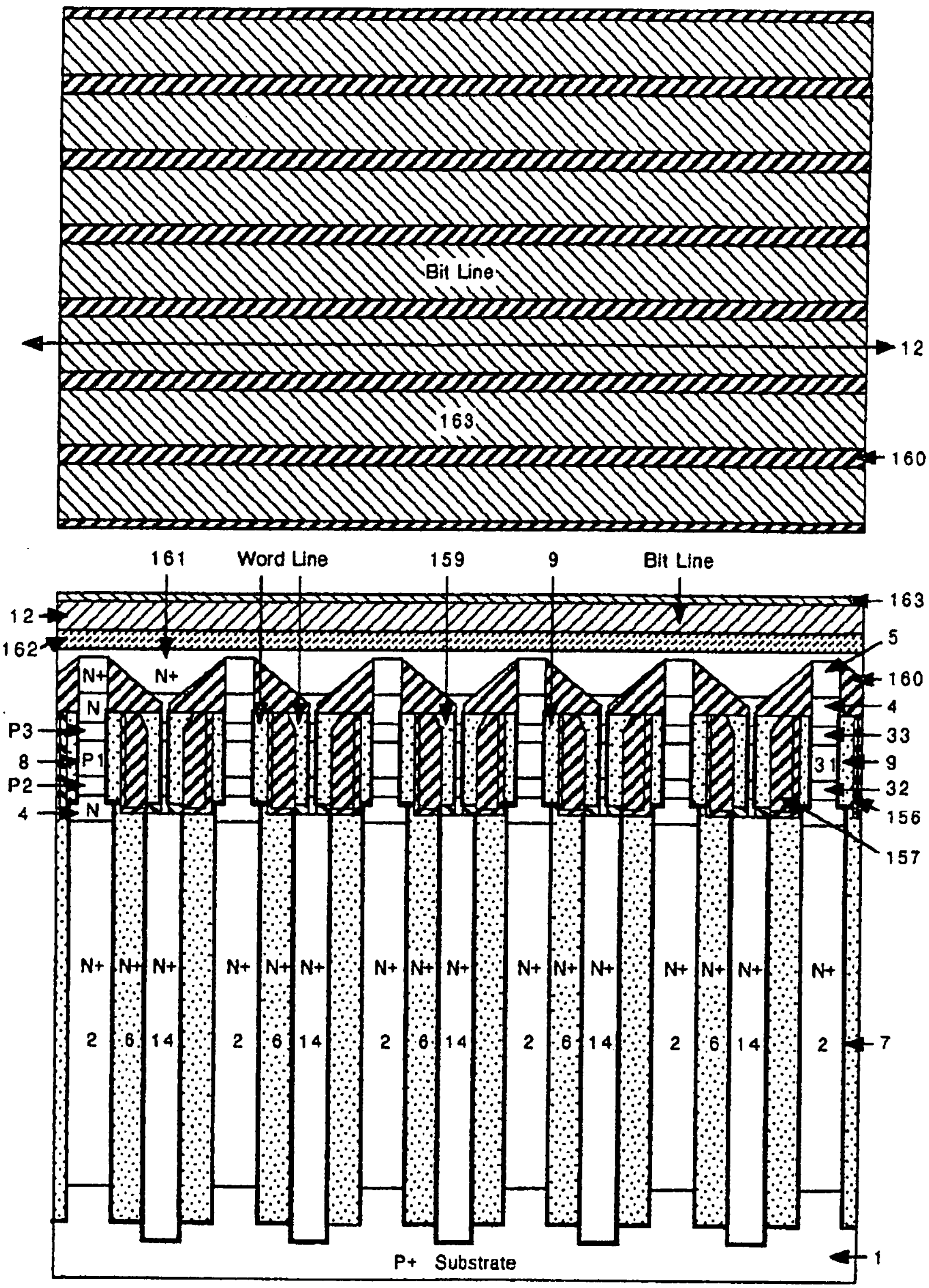
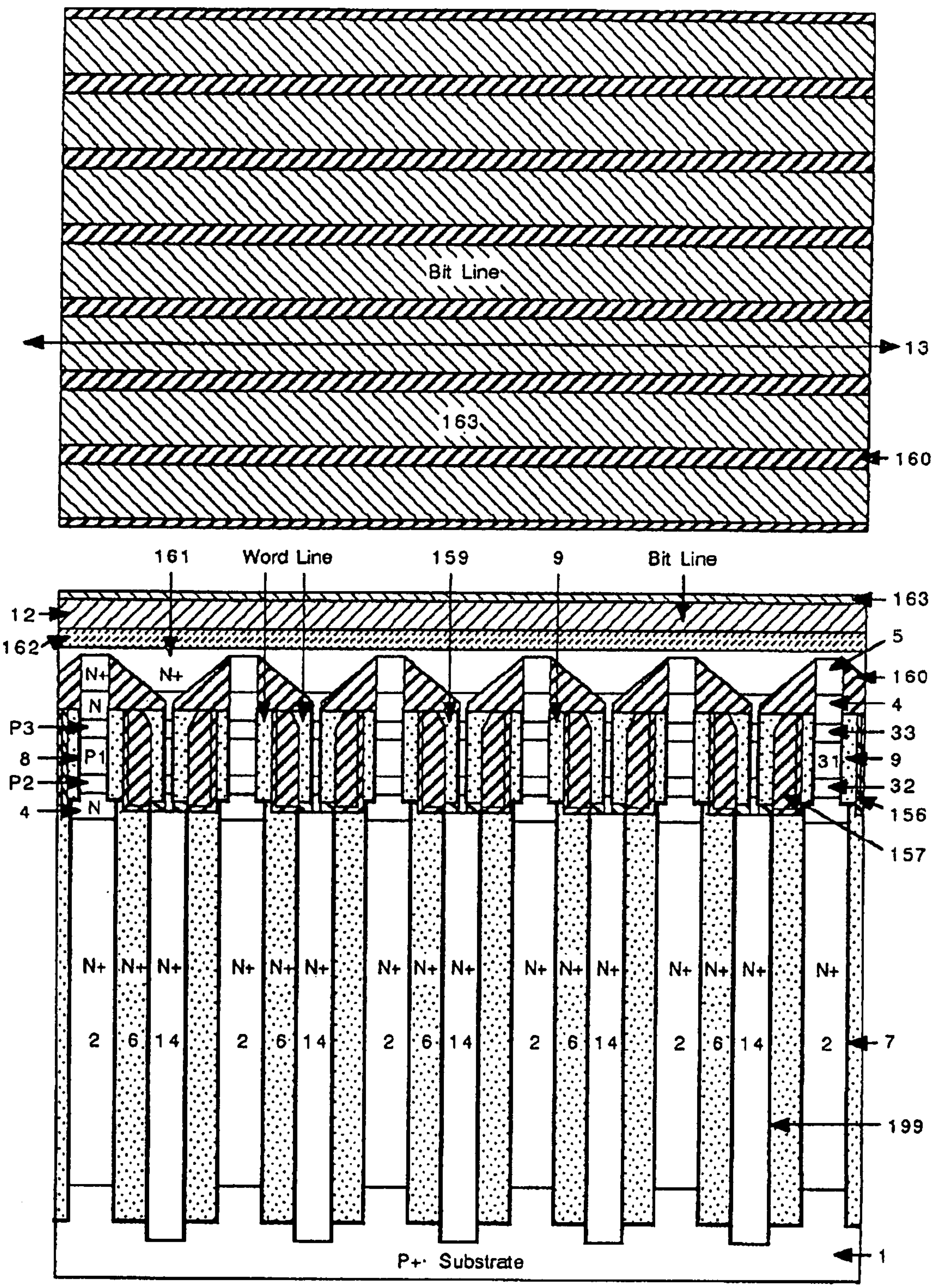

Bit Line
12
163
160
161
Word Line
159
9
Bit Line
163
12
162
5
N+
N+
160
N
4
P3
33
8
P1
9
P2
31
32
4
N
156
157
N+
2
6
14
7
P+ Substrate
1

Fig.12



Bit Line
13
163
160
161
Word Line
159
9
Bit Line
163
12
162
5
N+
N+
160
N
4
P3
33
8
P1
31
9
P2
32
4
N
156
157
N+
N+
N+
N+
N+
N+
N+
N+
N+
N+
N+
N+
N+
N+
N+
N+
2
6
14
2
6
14
2
6
14
2
6
14
2
6
14
2
7
199
P+ Substrate
1

Fig.13

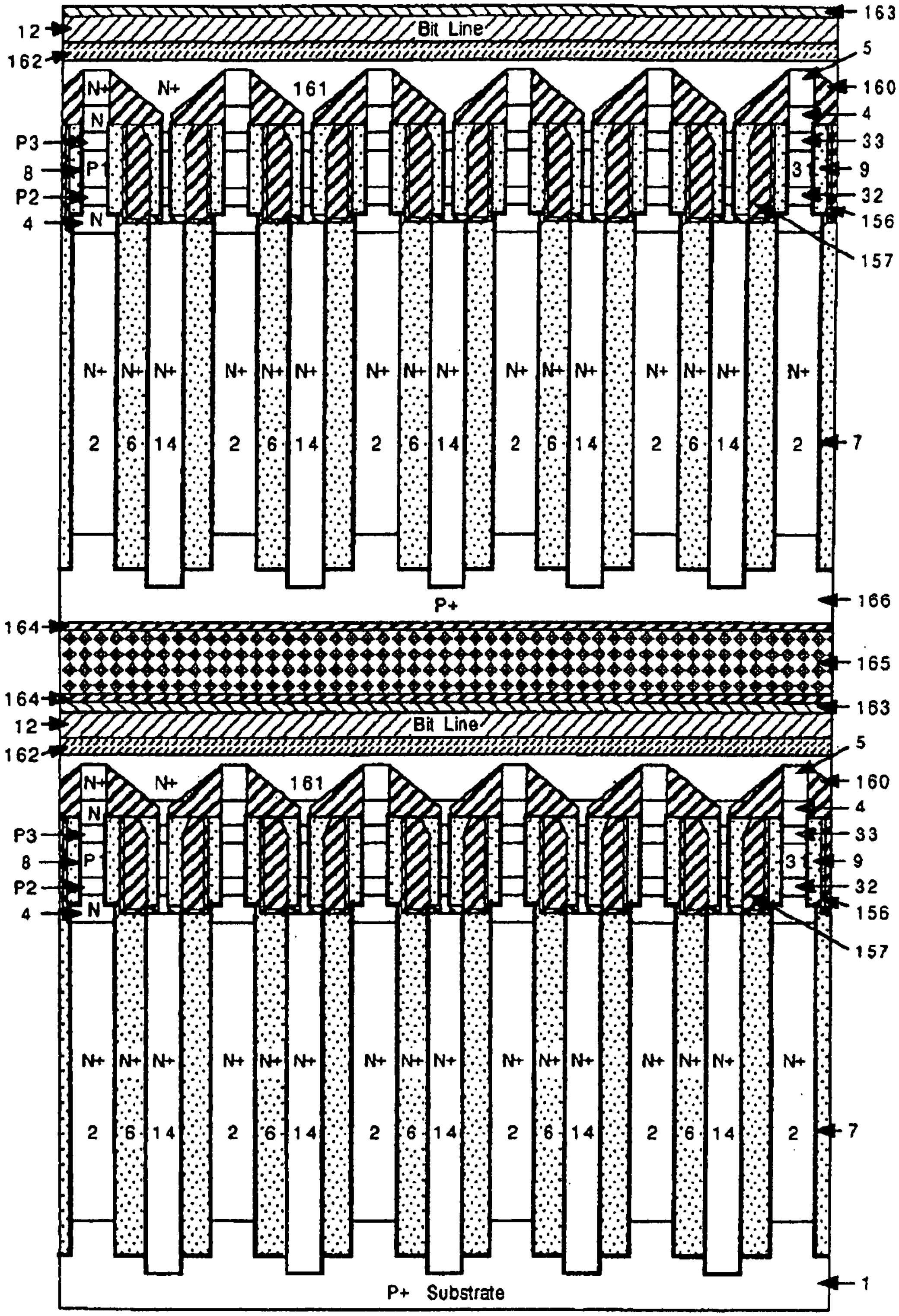

Bit Line
12
162
163
5
160
161
N+
N
P3
8
P
P2
4
33
9
32
156
157
2
6
14
7
P+
166
164
165
P+ Substrate
1

Fig.14

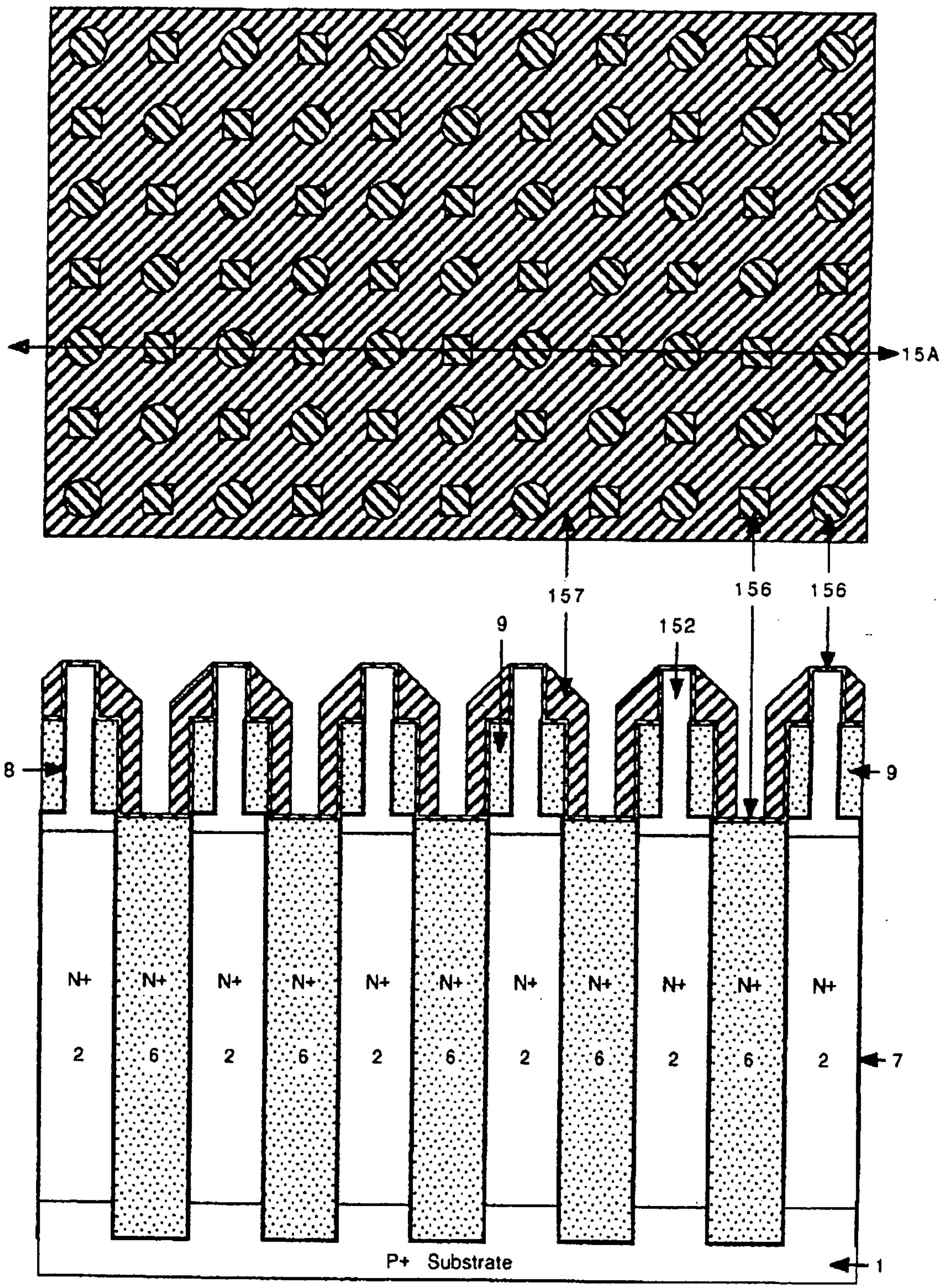


Fig.15A

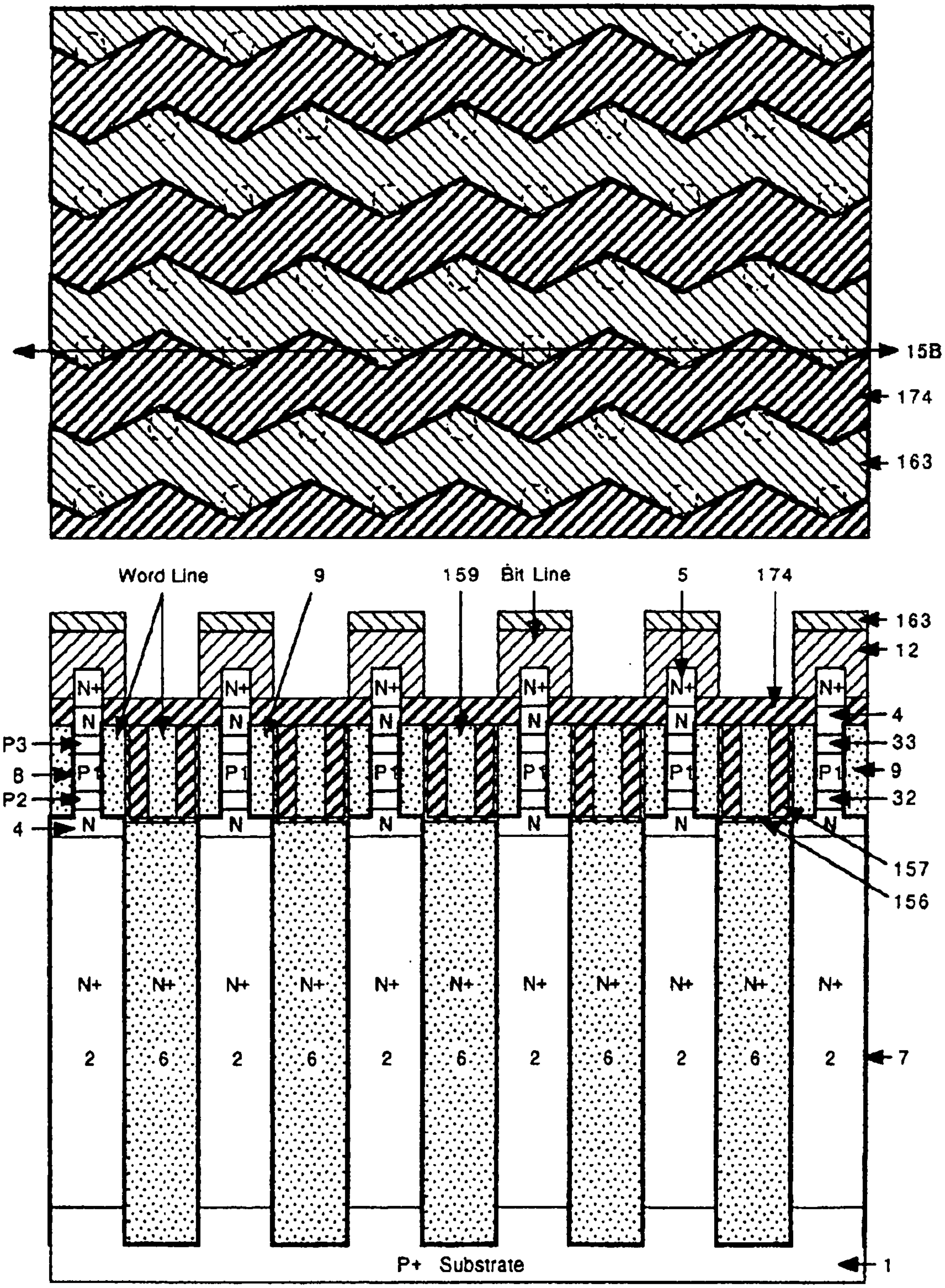

15B
174
163
Word Line
9
159
Bit Line
5
174
163
12
N+
N
P3
8
P1
P2
4
33
9
32
157
156
N+
2
6
7
P+ Substrate
1

Fig.15B

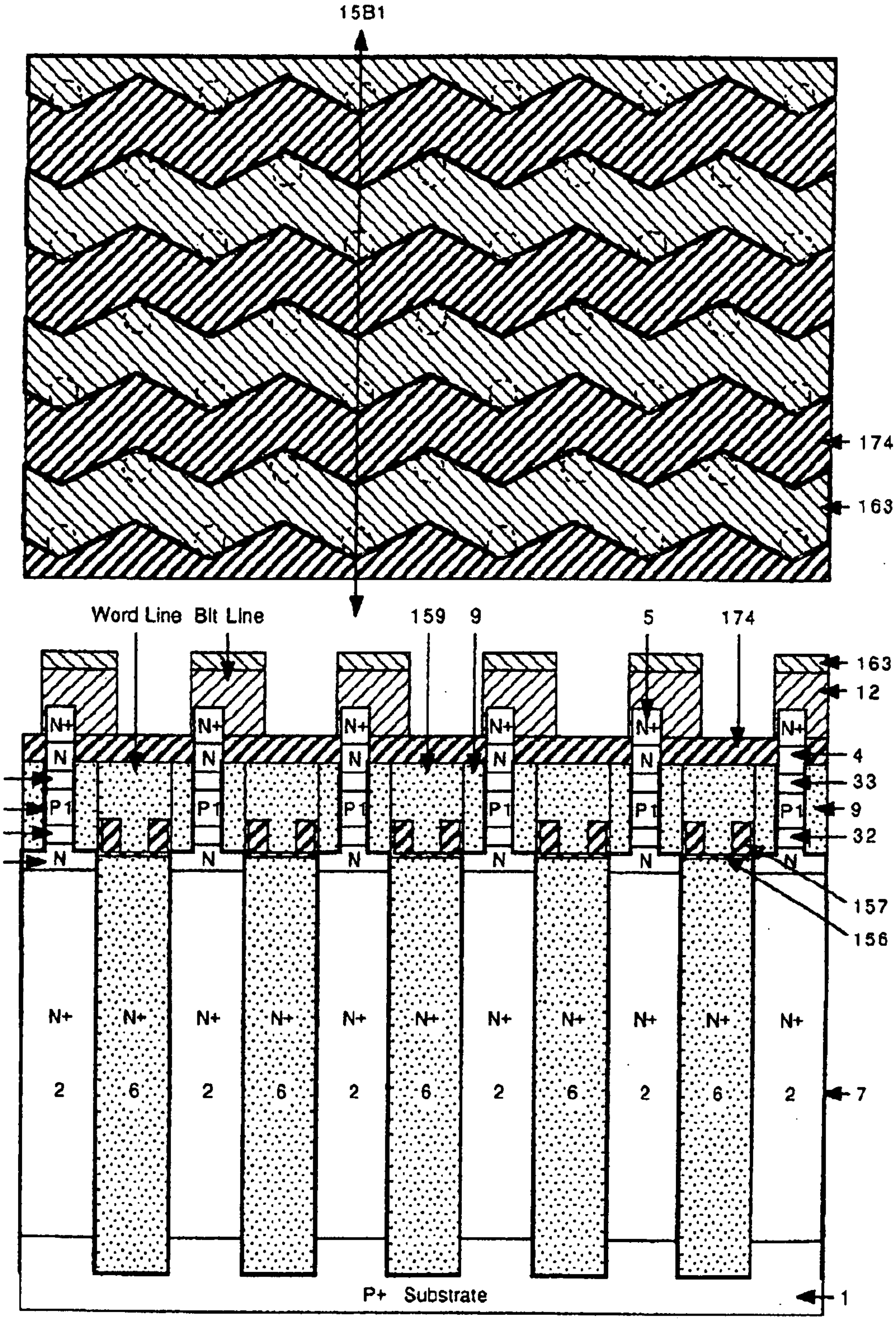

15B1
174
163
Word Line
Bit Line
159
9
5
174
163
12
N+
N
P3
8
P1
P2
4
33
9
32
157
156
N+
2
6
7
P+ Substrate
1

Fig.15B1

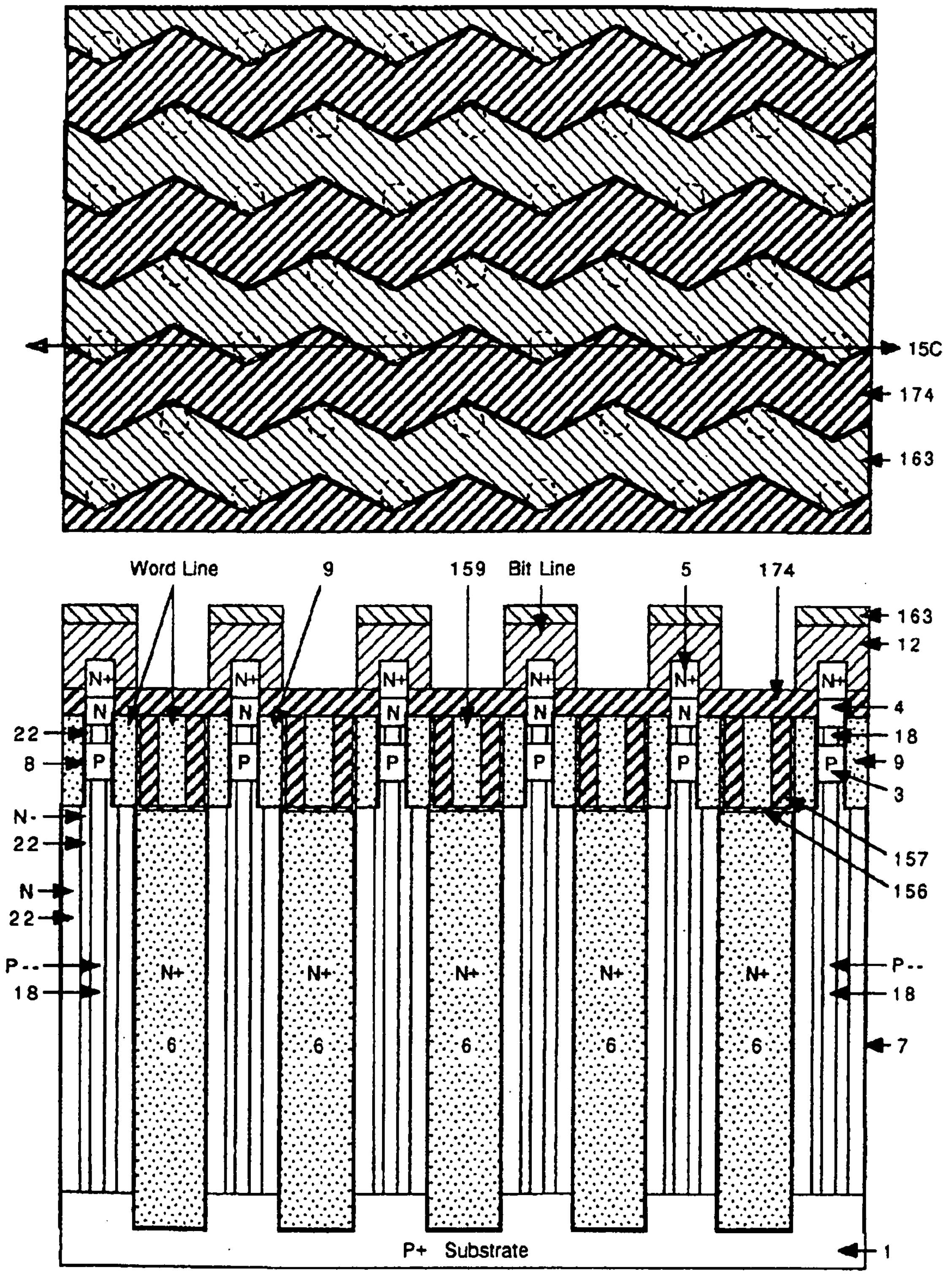

15C
174
163
Word Line
9
159
Bit Line
5
174
163
12
N+
N
P
4
18
9
3
22
8
N-
22
N
22
P--
18
N+
6
157
156
P--
18
7
P+ Substrate
1

Fig.15C

1　Ａｂｓｔｒａｃｔ

Ultra dense integrated circuits including a dynamic random access memory (DRAM) array with a minimum 1 lithographic square cell size and a 6 transistor CMOS static random access memory (SRAM) cell with a minimum of 40 lithographic squares can be formed by a novel vertical transistor named Buried Gate Transistor (BGT). The BGT has less short channel effect, higher reliability and reproducibility, and better device uniformity than any other vertical transistor; the BGT has higher performance (or higher current drivability) and higher density than any advanced planar transistor because the BGT has a larger effective channel width even in a small occupied area. Second, the problem of limitation in the channel length imposed by lithography is overcome. Third, the BGT has higher immunity against misregistration and higher yield than any conventional device. Therefore, the BGT is superior to any other transistor in the world.

2　Ｒｐｅｓｅｎｔａｔｉｖｅ　Ｄｒａｗｉｎｇｓ

Ｆｉｇ．１